AS Electronic textbook

By Ian Kemp with additions for City and Islington Sixth Form College

INTRODUCTION

This support booklet is written for candidates following the AQA Electronics specification. It is not intended that it should be a rigorous academic text, but rather that it should provide candidates and teachers with a working knowledge of the Electronics covered by this module of the specification. This booklet should be used in conjunction with the specification. It is assumed that candidates will have a knowledge and understanding of Electronics as defined in the National Curriculum for Science up to, and including level 7.
In the Unit test candidates will be expected to draw appropriate circuit diagrams and perform calculations using the equations as given on the Data sheet in the specification.

Throughout this booklet the numbering system for each section is the same as that used in the subject specification.

I am grateful for the help and advice given by Terry Williams, Stuart Wisher, David Neal and Tim Kemp in the preparation of this booklet.

OVERVIEW OF THE FOUNDATION ELECTRONICS MODULE SPECIFICATION

The module starts with an introduction to electronic systems as the basis for all of the electronics that is considered within the Specification. It introduces the concept that a simple system consists of an input, a processing element, an output and possibly some feedback control. All complex systems can be broken down into simple sub-systems with the above form.

Before electronic systems can be assembled it is necessary to understand something of the elements of a subsystem. Logic gates are therefore introduced as 'processing elements' for simple systems and the truth tables of the six basic logic gates are covered. Combinations of these gates can be easily formed to create complex systems. As the number of gates increases it is possible to simplify and rationalise circuits by considering the Boolean algebra expressions of the system. It is assumed that only very high input impedance logic gates (CMOS, HC, HCT series etc) will be used.

To enable an output to be obtained from a logic system, LEDs are introduced along with the necessary calculations involving electrical power and Ohm's law in order to calculate the series resistances for the LEDs. Silicon diodes are also introduced as a convenient way of increasing the number of inputs on a logic gate, as well as their more general properties and applications. The zener diode provides a quick and convenient way of stabilising a power supply to enable logic gates to be operated.

Resistive input transducers in the form of light dependent resistors and thermistors are now introduced as input devices to the logic gate processors already covered. In order to successfully use a resistive input device it is necessary to incorporate it into a voltage divider. Suitable calculations and graphs of the output voltage from such arrangements are considered.

The systems that can be constructed so far will only operate LEDs, the logic gates not being able to supply sufficient current to operate any larger devices. Therefore to expand the range of systems, transistors and MOSFETs are now covered. Their function is restricted to

behaving as a switch, so enabling logic gates to control high power devices. The advantages and disadvantages of modern MOSFETs over transistors become apparent with practical applications.

With the addition of transistors and MOSFET devices to electronic systems, large currents can be controlled and so some common output devices can now be introduced. Many of these devices are electromagnetic and so the output switching device (transistor or MOSFET) needs to be protected, using a diode, from the large voltage produced when the device is switched off. Relays, themselves, are also considered as important output switching devices because of the way in which they will switch substantial currents and voltages, and yet provide complete isolation from the main electronic circuit.

While logic gates will act as processors in analogue switching circuits, their function is limited. Operational amplifiers are much more suited to this role and so are introduced as comparators. The differences in operation between real and ideal op-amps will need to be considered as theoretical circuits are constructed with real components.

All the systems produced so far will have an output that changes immediately that an appropriate input change occurs. In some applications this is undesirable and so capacitors

are introduced as a means of introducing a delay or timing function into electronic systems. Knowledge of time constants and charging / discharging graphs will enable timing delays to be determined.

Time delays produced in this way lack precision. This can be remedied by using a 555 timer IC in monostable mode. A 555 timer will also function as a pulse producer (astable) and so can be used to generate audible tones and flash lamps, which can be used as output devices.

OVERVIEW OF THE FURTHER ELECTRONICS MODULE SPECIFICATION

This module develops and extends the ideas and concepts introduced in the Foundation Electronics module so that candidates have a more comprehensive knowledge of basic electronic circuits that can then be applied to the coursework projects.

The module starts by briefly reviewing the digital electronics and logic concepts introduced in the Foundation module and then extending them into a more detailed study of Boolean Algebra and the minimisation of logic circuits as they are developed. To aid the minimisation process, Karnaugh maps are introduced and examples used to show their application. In examination questions, candidates will be allowed to decide whether they use Boolean Algebra or Karnaugh maps for the minimisation process.

All combinational logic systems process the information immediately (apart from the transition time within the gate). While this can be desirable, there are many situations where it is desirable for information passed into the logic system to be processed sequentially or after a delay. The section introduces the D type flip-flop and shows how they can be combined into counters, latches and shift registers. Monostables and astables are also revisited from the Foundation module at which stage they were constructed using the 555timer IC. In this module they are constructed from NAND gates together with the mathematics required to estimate the timing period. The specification assumes that all logic circuits have a very large

input resistance and a low output resistance as found in CMOS and high speed CMOS ICs. (4xxx, 74HCxxx and 74HCTxxx series), and it is strongly recommended that these devices are used in all practical work.

Binary and modulo-n counters are then introduced along with the conversion of numbers between binary, decimal and hexadecimal notations. Numbers are restricted in this module to four bits only and although details are included of how to convert larger numbers, since the method will be needed for module 3, many candidates may choose simply to learn the conversion table instead. Consideration is also given of how to display numbers on a seven segment array. In the majority of cases the decoding of binary coded decimal (BCD) numbers for the display is carried out using dedicated ICs.

Operational amplifiers were introduced in the Foundation module as effective comparators. In this module they are used as amplifiers in inverting, non inverting, summing and buffer modes by employing negative feedback to reduce the closed loop gain of the system. Consideration is given of how the gain of these amplifiers can be calculated along with the bandwidth that can be expected. The relationship between bandwidth and gain is investigated. All op-amp circuits are based on devices with a very large input resistance, as found in the BiFET range of op-amps ie, TL071, TL081 etc.

Capacitors have already been considered in the Foundation Module as part of timing systems. They are now considered as components in ac circuits to form frequency dependent circuits when combined with resistors. Such passive first order filters are discussed in some detail along with the mathematics required to estimate the 'break points' of the filters. Both low pass and high pass filters are described and their application to treble boost, treble cut, bass boost and bass boost circuits considered.
Frequency selective elements can also be included in op-amp amplifier circuits to form active filters. Consideration is given of how to design first order filters to custom specification, so that they can be used to tailor the frequency response of an amplifier to that required.

The last element of the module deals with how to obtain sufficient power to operate a loudspeaker from an op-ampMOSFET source followers form the basis of this topic and are configured in a complementary push-pull arrangement. Push-pull circuits while having lower power losses than single device output circuits do suffer from cross-over distortion. This is considered along with ways to minimise its effects.

All semiconductor devices passing significant current, generate heat internally. For the safety of the device, this heat has to be removed to ensure that it does not get too hot. This is achieved by mounting the device onto a heatsink. The design and construction of heatsinks is considered along with the necessary mathematics to estimate the required size of heatsink, based on the power being dissipated by the device.

All elements in this module link directly to the sub-systems that form the building blocks of any electronic system and it would be helpful to candidates if they considered this aspect as each element of the module is studied.

CONTENTS

10.1   SYSTEM SYNTHESIS

The electronics revolution that has happened within the last forty years has not been brought about by the development of new electronic circuits. Indeed, the vast majority of all modern complex electronic systems consist of circuits that were developed within the last sixty years. The revolution that has brought about the great advances in electronics is two fold:

      (a)   the ability to manufacture large silicon crystals of exceptional purity and

      (b)   the ability to fabricate extremely complex circuits, using photographic techniques, into an Integrated Circuit, IC.

This has led to very complex circuits being available which are very cheap, very small and very reliable. The latest microprocessors have in excess of four million transistors fabricated onto a piece of silicon approximately 1cm^2, and yet cost as little as £20. Analysis of the circuit diagrams of even such complex systems as microprocessors reveals that they are made from many smaller sub-systems that had been developed a long time ago. Analysing complex electronic systems into subsystems that can be recognised and understood is a vital part of modern electronics. It is for this reason that the 'Systems' approach to electronics is fundamental to this Electronics course.

All electronic systems can be analysed into small, discrete sub-systems which will, in general, consist of the following sections:-

- an input,
- a processor,
- an output,
- and possibly some feedback.

Using this concept, complex electronic systems can be broken up into smaller and simpler sub-systems, where each section is represented by a labelled box and the lines between the sections represent the flow of information. A typical example is shown below in figure 1.1. The arrows indicate the flow of information through the system.
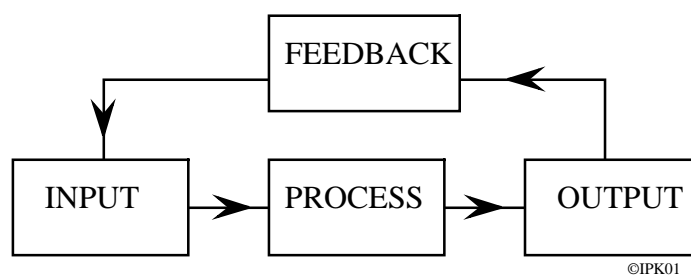
Figure 1.1

As an example, consider a security lamp which will switch on a high powered mains lamp for a preset time when it detects the movement of a warm object and the external lighting level is below a preset value. Both the time and the external light level can be preset by the owner. Figure 1.2 shows how such a complex system can be analysed into basic sub-systems. These sub-systems can then be analysed into even more basic sub-systems. For example the light level sensor can be separated into three simpler sections, the LDR light sensor, the voltage divider and the darkness control, which allows the user to set the light level above which the lamp does not light.
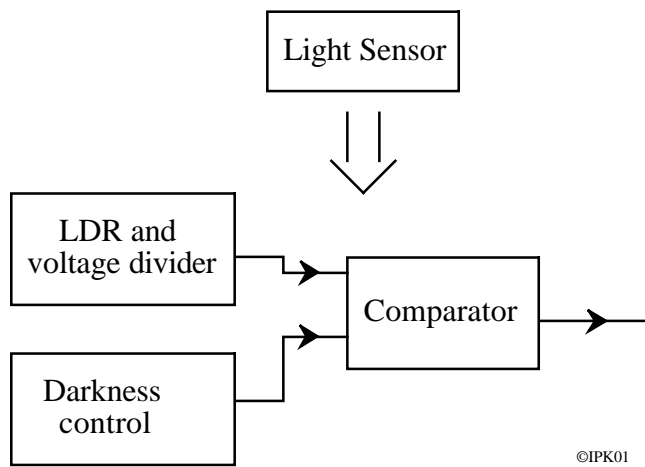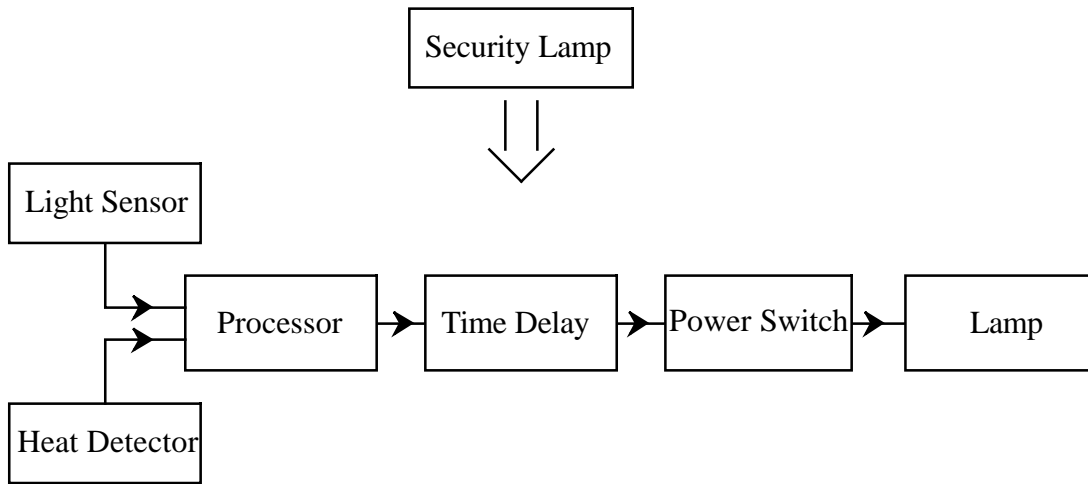
Fig 1.2

Electronic systems are only able to process information if the information is first changed into electrical signals representing that information. This is the function of the input device or *transducer*. There are many different types of input device. Some will actually generate an electrical signal, eg a dynamic microphone and a photodiode. Others rely on a change of their properties (eg resistance) to cause a change in an electrical circuit, for example, an LDR (Light Dependent Resistor) or a thermistor.

Some more examples of different input transducers are shown below in figure 1.3.
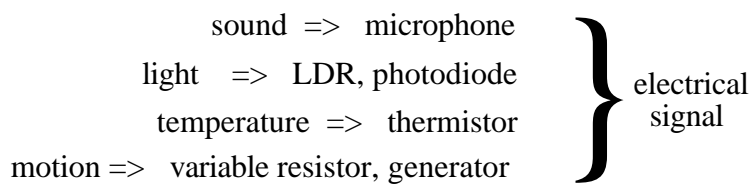
Figure 1.3

There are many different types of basic processing that can be carried out by the processor in an electronic system. These include the following, many of which are covered in other modules of this GCE course.

Amplifying
Analogue to Digital Conversion
Comparison
Digital to Analogue Conversion
Equalisation
Logical Operations
Memorising signals
Signal limiting
Timing

Once the electronic system has processed the information, the electrical signals need to be changed back into a form that is usable by the outside world. This is the purpose of the output device or transducer, some examples of which are shown below in figure 1.4.

$$
\text{electrical signal} \left\{ \begin{array}{l}
\text{sound} \Rightarrow \text{loudspeaker} \\
\text{light} \Rightarrow \text{lamp, LED, television screen} \\
\text{heat} \Rightarrow \text{resistor} \\
\text{motion} \Rightarrow \text{motor, electromagnetic solenoid}
\end{array} \right.
$$
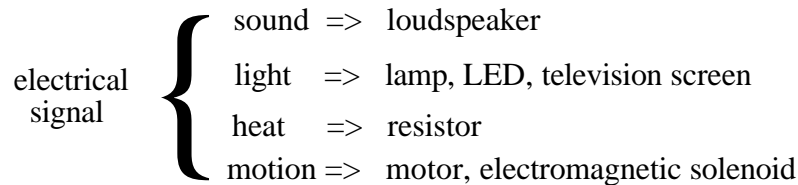
Figure 1.4

As a design exercise, consider a system to maintain a preset, constant temperature in a room.

In keeping with all electronic systems, input transducers, a processor and a output transducer are required.

One input transducer needs to change temperature into an electrical signal and so a *thermistor* could be used.

A second input transducer needs to give an electrical signal from the preset temperature control. A *variable resistor* could be used for this application.

The processor will need to compare the electrical signal from the input transducers and so a *comparator* could be used.

The output transducer will need to convert electrical signals back into heat, which could be achieved using a high power resistor.

This system will also have feedback since as the resistor heats the air in the room, the change in temperature of the air will be fed back to the input transducer.

As a design exercise, try to draw a system diagram for the system described above.

10.2   LOGIC GATES AND BOOLEAN ALGEBRA

There are many different logic operations that can be incorporated into a **processor**, resulting in the output transducer responding in a defined way to the state of the various input signals. The actual function of a logic processor is defined by a **TRUTH TABLE** which will summarise **ALL** possible output states for **ALL** possible combinations of input states. Analogue electronics uses continuously varying voltages and so it is not possible to produce tables showing the relationship between every possible input and output since such tables would be infinitely long.

Consider an example of an electronic system.

> *A car manufacturer wants to incorporate a seat belt alarm to warn the driver when the seat belt is not fastened. The alarm must sound when the ignition is switched on, the driver is sitting in the driver's seat and the seat belt is not fastened. The manufacturer fits switches into the seat and seat belt.*

This is an ideal problem to solve with a Digital electronic system. Digital electronics is concerned with switching-type circuits in which the inputs and outputs involve only two levels of voltage (or current). Digital information (signals) therefore consists of a series of voltage pulses, with a **HIGH** voltage being represented by a **1** and a **LOW** voltage being represented by a **0**.

Digital circuits consist of **logic gates** which control the flow of digital information. A logic gate is a device which has one output and several inputs. The output will either be a logic 1 (high) or a logic 0 (low) depending on the input signals. The logic gates covered in the specification are assumed to have a very high input resistance, and a low output resistance. Logic 0 is assumed to be less than half of the supply voltage and logic 1 is assumed to be more than half of the supply voltage. These are the characteristics of the CMOS, 74HC and 74HCT logic families. All of these logic circuits will operate from a well regulated +5V supply and it is assumed in circuit diagrams that a power supply is connected even though the connections will not be shown.

In the example given above, the information needs to be changed into electrical signals. This is the task of the seat switch, the ignition switch and the seat belt switch. These are wired so that the following signals are produced.

> The seat switch gives a logic 0 when the seat is occupied and a logic 1 when it is unoccupied.
> The seat belt switch gives a logic 0 if it is fastened and a logic 1 if it is unfastened.
> If the ignition switch is on then it gives a logic 1.
> The alarm needs a logic 1 to sound.

The alarm is therefore to sound if
> the ignition switch is on, (1),
> the seat belt is unfastened, (1),
> and the seat is occupied, (0).

This information can be neatly summarised in a Truth Table for the system showing all of the possible input states.

IGNITION SWITCH	SEAT BELT SWITCH	SEAT SWITCH	ALARM
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	**1**	**0**	**1**
1	1	1	0

Before converting this truth table into an electronic circuit it is necessary to consider the three basic logic gates of **AND**, **OR** and **NOT** together with simple combinations which form **NAND, NOR** and **EX-OR** gates.

All digital electronic circuits are built from combinations of these basic gates.
Although only two input AND and OR gates are shown below, the same principal applies to these gates if they have many inputs.

The truth table and logic symbol for a two input AND gate is shown in figure 2.1.

Therefore the output of an **AND** gate is a 1 if input A *AND* input B are both 1.

INPUTS
A
B
AND
OUTPUT
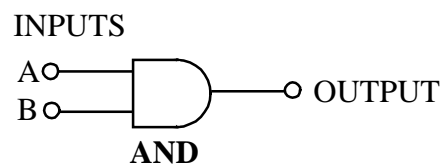
A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

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Figure 2.1

The truth table and logic symbol for a two input OR gate is shown in figure 2.2
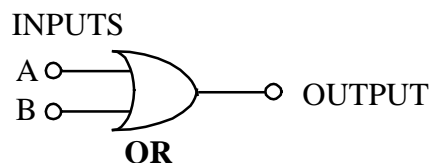
INPUTS
A
B
OR
OUTPUT

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

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Figure 2.2

Therefore the output of an **OR** gate is a 1 if input A *OR* input B is 1.

The truth table and logic symbol for a NOT gate is shown in figure 2.3.
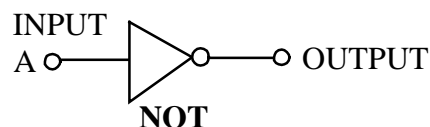
INPUT
A
NOT
OUTPUT

A	OUT
0	1
1	0

©IPK01

Figure 2.3

Therefore the output of a **NOT** gate is always the opposite of its input.

From these basic gates more complex ones can be constructed, the most common of these being the **NAND** and **NOR** gates. The logic symbols and truth tables for these gates are shown in figures 2.4 and 2.5.

INPUTS A B **NAND**

A B OUTPUT **NAND**

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Figure 2.4

INPUTS A B **NOR** OUTPUT

A B OUTPUT **NOR**

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0
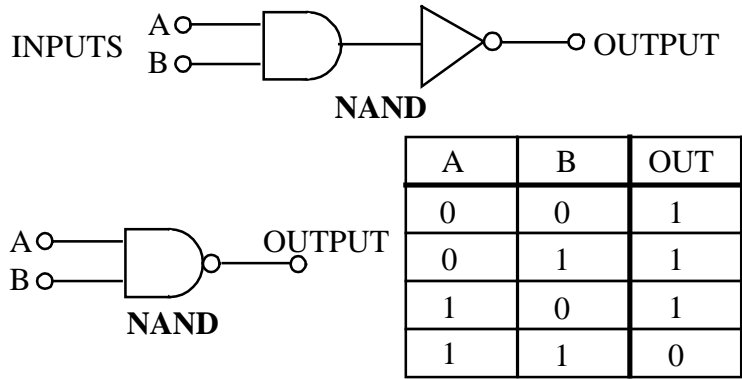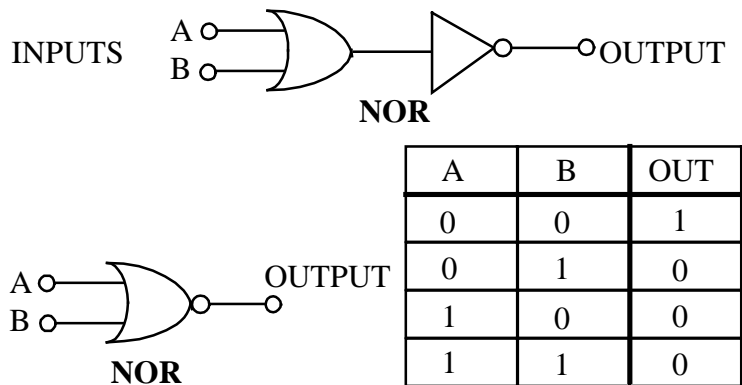
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Figure 2.5

Many other logic circuits can be produced using the five logic gates described so far and a technique is needed to analyse such circuits. This is most easily described using an example.

Consider the logic circuit shown in figure 2.6.
The output of each gate is recorded as a separate column in the truth table. In this way, inputs A and B give the intermediate outputs C and D, which in turn, form the inputs for the final AND gate.

INPUTS A B C D OUTPUT

A	B	C	D	OUT
0	0	1	0	0
0	1	1	1	1
1	0	1	1	1
1	1	0	1	0
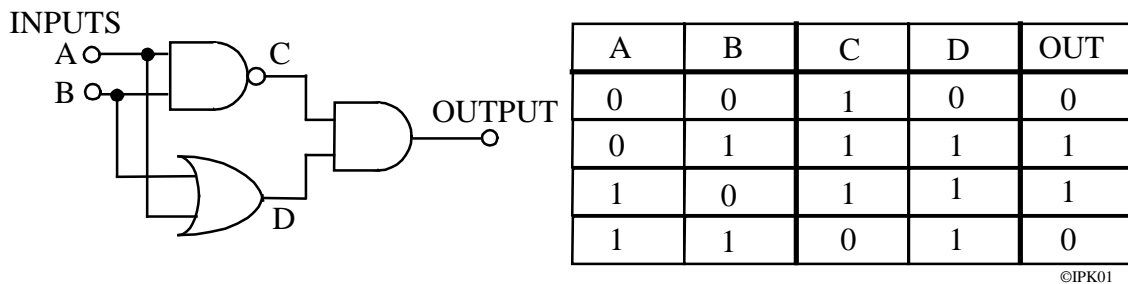
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Figure 2.6

This logic circuit functions as a digital comparator in that when the two inputs are the same the output is a logic 0 and when the two inputs are different the output is a logic 1. This function is very useful and is often required in complex logic circuits (it forms the basis of a binary addition circuit). It is given the name of **Exclusive-OR** and is fabricated as a single logic gate with the circuit symbol and truth table shown in figure 2.7.

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

©IPK01
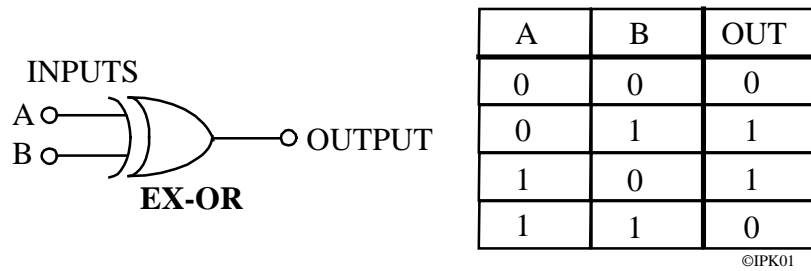
Figure 2.7

With the basic logic gates now available, the truth table for the seat belt alarm from page 11 can now be converted into logic gates. Looking at the truth tables for the basic logic gates it can be seen that the truth table for the seat belt alarm is similar to that for a three input AND gate in that there is only one input combination that gives a logic 1 output. The next task is to consider how this could therefore be made using an AND gate. A little thought will show that if the SEAT SWITCH output is inverted by passing it into a NOT gate, then an AND gate can be used to combine the three inputs.

The resulting circuit diagram is shown in figure 2.8.
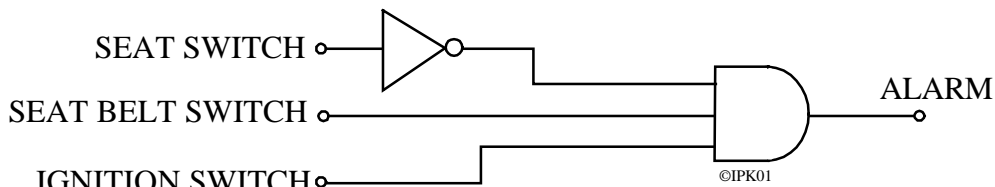
Figure 2.8

Three input AND gates are not as common as two input NAND gates and so it is a useful exercise to redesign the circuit using just two input NAND gates.

A NOT gate can be made from a two input NAND gate with both of its inputs connected together. An AND gate can be made from a NAND gate followed by a NOT gate. The seat switch and the seat belt switch can therefore be combined using the circuit shown in figure 2.9.
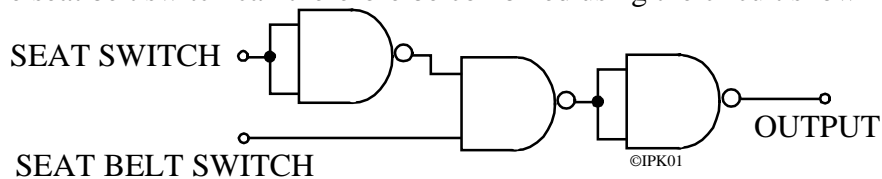
Figure 2.9

Also the alarm must sound only when the ignition switch is on, i.e. at logic 1, **AND** when the output from the previous circuit is also a logic 1. These two signals can therefore be combined using another AND gate made from two NAND gates, one wired as a NOT gate. The complete circuit is shown in figure 2.10.
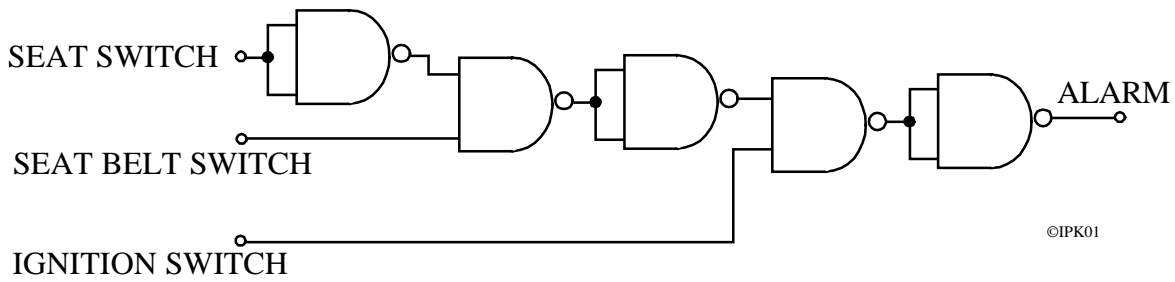
Figure 2.10

This circuit appears to be much more complicated than the circuit shown in figure 2.8. However, logic gates are supplied as Integrated Circuits (ICs), each IC usually containing several identical gates. Two input NAND gates are supplied in an IC containing four such gates and so it is economically advisable to use as many of the gates as possible rather than several ICs each containing different logic gates.

It is a useful exercise to work out how to form the following logic functions:-
    a NOT gate from a NOR gate,
    a NOT gate from an EX-OR gate,
    an AND gate from three NOR gates,
    an OR gate from three NAND gates,
    an EX-OR gate from four NAND gates.

Boolean Algebra

Logic circuits may be described by following a notation developed by George Boole in 1847 which was originally used to compare logical word statements. It was first used in electronic systems in 1938 when it was adapted by Claude Shannon to describe telephone switching systems and it is in this form that it is used today. Boolean algebra is a shorthand way of writing logic statements. Some of the more common logic statements are shown below.

A = B   means 'the logic state of A is the same as the logic state of B'
                          ie when A is 1, B is 1 and when A is 0, B is 0.

A + B = Q   means 'output Q is 1 when input A is 1 **OR** input B is 1'.
   **Note:** the + sign in Boolean algebra means **OR**.

A · B = Q   means 'output Q is 1 when input A is 1 **AND** input B is 1'.
                          Note: the · sign in Boolean algebra means **AND**.

$\overline{A}$ means 'NOT A'.
                          Note: a bar placed over an expression is read as **NOT**.

$\overline{A} = Q$ means 'output Q is 1 when input A is 0'.

$\overline{A + B} = Q$ means 'output Q is 1 when **N**either input A is 1 **OR** input B is 1'.
                          ie **NOR**.

$\overline{A · B} = Q$ means 'output Q is 1 when **N**either input A is 1 **AND** input B is 1'.
                          ie **NAND**.

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These logic statements can be used to express electronic circuits in terms of Boolean algebra expressions. Consider the circuit and truth table in figure 2.6 (which is reproduced below). This circuit behaved as an Ex-OR gate.

A	B	C	D	Q
0	0	1	0	0
0	1	1	1	1
1	0	1	1	1
1	1	0	1	0
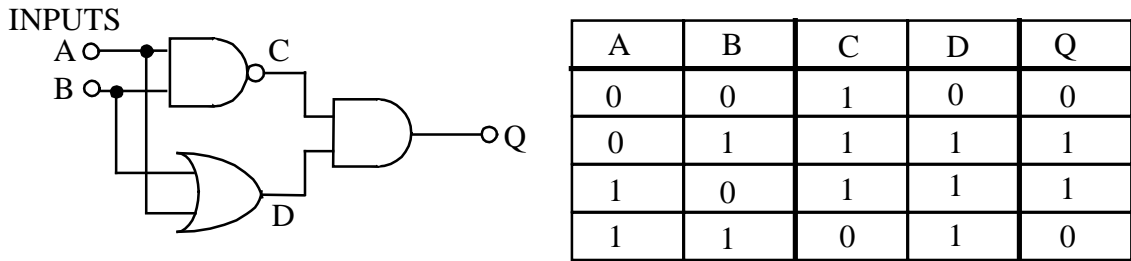
©IPK01

(Figure 2.6)

Output C can be written as $\qquad \mathbf{C = \overline{A \cdot B}}$

Output D can be written as $\qquad \mathbf{D = A + B}$

So the output Q can be written as $\qquad \mathbf{Q = C \cdot D = \left(\overline{A \cdot B}\right) \cdot (A + B)}$

Therefore the Boolean expression for Exclusive Or is $\mathbf{Q = \left(\overline{A \cdot B}\right) \cdot (A + B)}$

It can be shown that this expression simplifies to $\mathbf{Q = A \cdot \overline{B} + \overline{A} \cdot B}$

Since this is such a common and useful expression it is given its own Boolean algebra symbol,

$$\mathbf{Q = A \cdot \overline{B} + \overline{A} \cdot B = A \oplus B}$$

Boolean Algebra Laws

In order to be able to manipulate Boolean Algebra expressions it is necessary to consider the rules and laws that they obey. It can be shown, using truth tables, that Boolean Algebra expressions obeys the normal mathematical laws which are set out below.

Commutative Laws:
$$\mathbf{A + B = B + A}$$
$$\mathbf{A \cdot B = B \cdot A}$$

Associative Laws:
$$\mathbf{A + (B + C) = (A + B) + C}$$
$$\mathbf{A \cdot (B \cdot C) = (A \cdot B) \cdot C}$$

Distributive Law:
$$\mathbf{A \cdot (B + C) = A \cdot B + A \cdot C}$$

Boolean Identities

Some of the more common Boolean Identities are listed below. It is a worthwhile exercise to ensure that they can be verified.

$$A \cdot A = A$$
$$A + A = A$$
$$A \cdot \overline{A} = 0$$
$$A + \overline{A} = 1$$
$$A \cdot 1 = A$$
$$A + 1 = 1$$
$$A \cdot 0 = 0$$
$$A + 0 = A$$
$$A + A \cdot B = A$$
$$A \cdot (A + B) = A$$
$$\overline{\overline{A}} = A$$

Using Boolean Algebra

The main use of Boolean algebra is to simplify complex logic systems. This is required in AS Module 2. However, using the identities and laws, it is relatively straightforward to use Boolean algebra to verify the logic function of logic circuits. Consider the seat belt alarm system and the circuit diagram shown in figure 2.8 (which is reprinted below).

SEAT SWITCH (A)

SEAT BELT SWITCH (B)

IGNITION SWITCH (C)

ALARM

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(Figure 2.8)
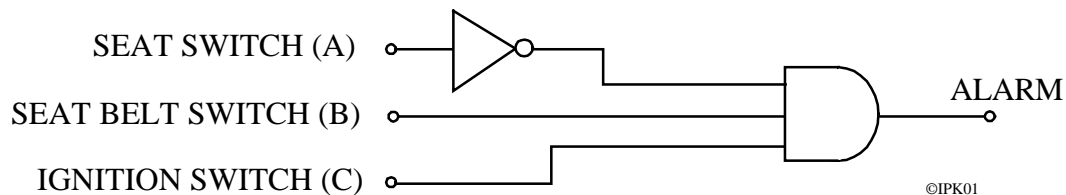
If **A** represents the input from the seat switch, **B** represents the input from the seat belt switch and **C** represents the input from the ignition switch, then the output **Q** can be written as

$$Q = \overline{A} \cdot B \cdot C$$

However, the circuit can also be constructed from two input NAND gates as shown in figure 2.10 (which is reprinted below).
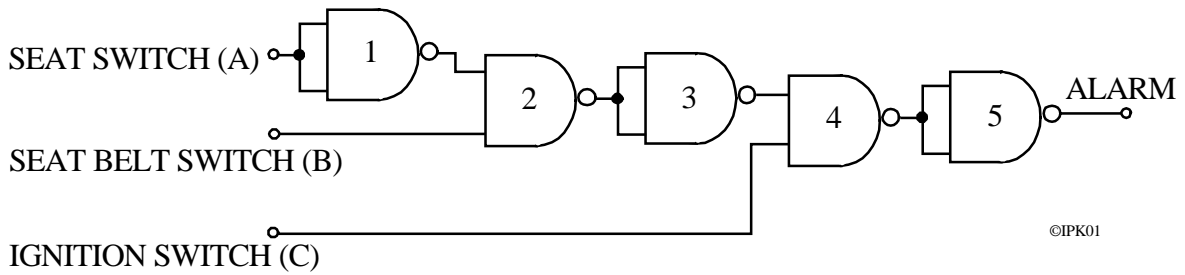
(figure 2.10)

Consider gate 1. The Boolean expression for the output is $\overline{A \cdot A}$
But using the identity $A \cdot A = A$ the equation simplifies to $\overline{A}$

Consider gate 2. The Boolean expression for the output is $\overline{\overline{A} \cdot B}$

Consider gate 3. The Boolean expression for the output is $\overline{\left(\overline{\overline{A} \cdot B}\right) \cdot \left(\overline{\overline{A} \cdot B}\right)}$

But using the identity $A \cdot A = A$ the equation simplifies to $\overline{\overline{\overline{A} \cdot B}}$
And using the identity $\overline{\overline{A}} = A$ the equation simplifies to $\overline{A} \cdot B$

Consider gate 4. The Boolean expression for the output is $\overline{\overline{A} \cdot B \cdot C}$

Consider gate 5. The Boolean expression for the output is $\overline{\left(\overline{\overline{A} \cdot B \cdot C}\right) \cdot \left(\overline{\overline{A} \cdot B \cdot C}\right)}$

But using the identity $A \cdot A = A$ the equation simplifies to $\overline{\left(\overline{\overline{A} \cdot B \cdot C}\right)}$
And using the identity $\overline{\overline{A}} = A$ the equation simplifies to $\overline{A} \cdot B \cdot C$

$$\Rightarrow Q = \overline{A} \cdot B \cdot C$$

which is the same as the expression for figure 2.8.

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10.3   CURRENT, VOLTAGE, POWER, RESISTANCE

In order for the processor of a system to interact with input and output transducers it is necessary to consider the basic properties of electricity.

Electricity is the effect of the movement of electric charge. The smallest quantity of electric charge possible is called an *electron.* The amount of electric charge each electron carries is very small and so very many electrons are involved in electric and electronic circuits.

Voltage can be thought of as being a measure of the *amount of energy* that the electrons moving in a circuit have. An electric current can be thought of as a *measure of the number* of electrons passing through a conductor.

If electrons are to move then they must have energy and so there can only be a current (flow of electrons) in a component when there is a voltage across it. If there is no voltage across a component, then there can be no current flow. However, it should also be remembered that if there is no path for electrons to pass through, then there will not be any current even though there may be a voltage difference.

It is important that all quantities used in electronics have appropriate units associated with them. The common units and their symbols are listed below.

Quantity	Unit	Symbol
voltage	volt	V
current	ampere	A
resistance	ohm	Ω
power	watt	W
frequency	hertz	Hz
capacitance	farad	F

These units are often too large or too small for given measurements. The farad is a very large unit; the capacitance of the Earth, when treated as a capacitor, is only a small fraction of a farad. On the other hand the ohm, when used in electronic circuits is very small and usually components with a resistance of many thousands of ohms are used. To simplify the use of these standard units, prefixes are used in front of them, just as they are with distance measurements, eg millimetre, kilometre etc.

Each of the common prefixes is shown below, together with one or more examples of units of magnitudes typically encountered in electronics.

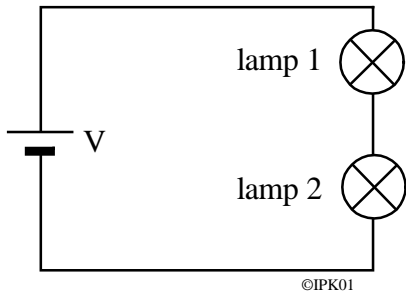|			
giga	×1,000,000,000	(G)	GHz
mega	×1,000,000	(M)	MHz, MΩ
kilo	×1,000	(k)	kHz, kΩ, kV
milli	×0.001	(m)	mV, mA, mW
micro	×0.000001	(μ)	μV, μA, μW, μF
nano	×0.000 000 001	(n)	nF
pico	×0.000 000 000 001	(p)	pF

Figure 3.1

There are essentially two ways in which electronic components can be arranged in a circuit, in **series** or **parallel**. A simple series circuit is shown in figure 3.1, consisting of a cell (battery) and two lamps.

As electrons pass around a circuit, they lose energy, but the electrons are **not** *"used up"* in any way. (Indeed, if they were, then the whole circuit would become radioactive!!) This means that in a series circuit the current will be the same wherever it is measured.

If three ammeters were placed in the series circuit as shown in figure 3.2, they would all have the same reading.
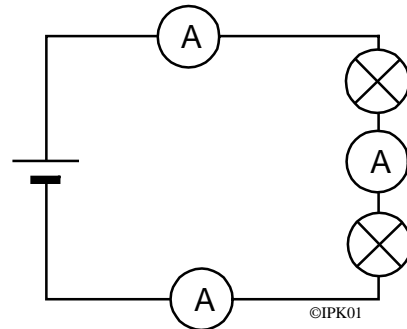
Figure 3.2

The same argument can also be applied to currents entering and leaving a junction in a circuit. Figure 3.3 shows a junction in a circuit. Since electrons cannot suddenly appear or disappear, the current shown on the ammeter must equal the sum of the other currents.
The ammeter therefore reads

$$3A + 2.2A - 1.5A = 3.7A$$

with the current flowing away from the junction.
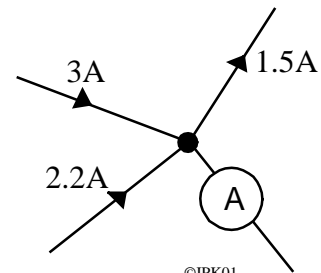
Figure 3.3

Electrons cannot give out any more energy in a circuit than they are initially supplied with by the power supply or battery. In a simple series circuit this means that the sum of the voltages across all of the components is equal to the voltage of the power supply. In figure 3.1 this means that

voltage across lamp 1 + voltage across lamp 2 = voltage of battery, V.

The only common circuit in which lamps are arranged in series is Christmas tree lights. There are usually twenty lamps connected together in series. Each lamp is rated at 12V and so the whole series circuit can be connected to the mains electricity supply of 240V (230V).
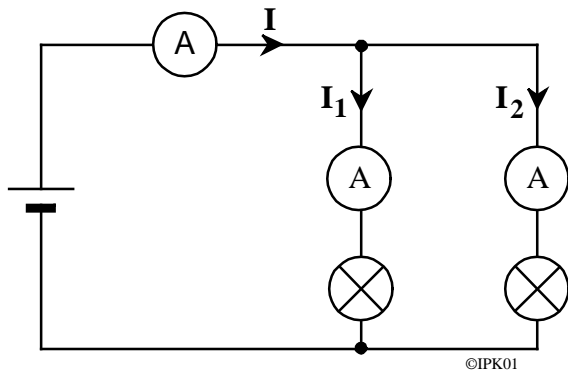
A simple parallel circuit is shown in figure 3.4. As can be seen, each lamp is connected directly (through an ammeter) to the battery, and so the voltage across each lamp is the same as the battery voltage.

The current, however, is split at each junction. This means that

$$I = I_1 + I_2$$

Figure 3.4

Ohm's Law

Electrons move more easily through some materials than others when a voltage is applied across the material. The opposition to current flow is called **resistance** and is measured in **ohms (Ω)**. Larger units are *kilohm*, ($k\Omega = 10^3 \, \Omega$) and *megohm*, ($M\Omega = 10^6 \, \Omega$.)

Resistance is defined as follows.

$$\mathbf{resis\,tan\,ce = \frac{voltage}{current} = \frac{V}{I}}$$

The resistance will be measured in ohms when the voltage is in volts and the current is in amps.

This formula is often known as Ohm's Law and is probably the most important formula in electronics.

Ohm's law can be placed into a *Magic Triangle* to help with its re-arrangement.
The magic triangle is shown opposite.
To find a formula, cover up the letter that you require and the formula can be read from the triangle.
eg, to find I, cover the letter I and then I = V/R.
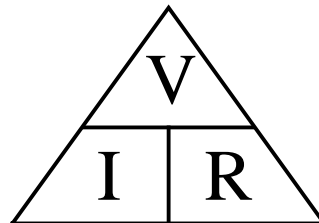
Example

A resistor has a voltage of 25V across it and a current of 0.5A passing through it.
What is the resistance of the resistor?

$$\mathbf{resis\,tan\,ce = \frac{voltage}{current} = \frac{25}{0.5} = 50\Omega}$$

Resistors In Series
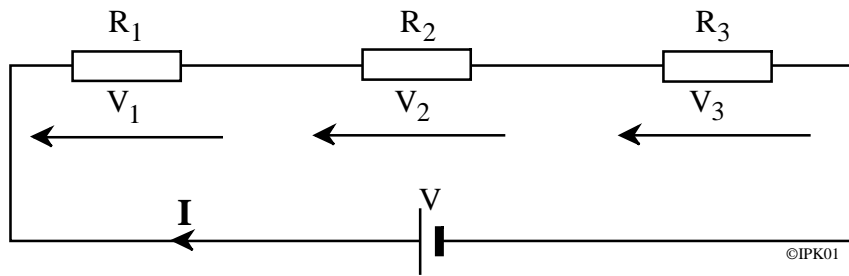
Figure 3.5

When several resistors, eg. R_1, R_2, and R_3 are connected in series, as in figure 3.5,

- the same current, **I**, passes through each resistor,

- the applied voltage, **V**, is equal to the sum of the voltages across the separate resistors :

$$\Rightarrow V = V_1 + V_2 + V_3$$

- the total resistance, **R,** is the sum of the separate resistors.

$$\Rightarrow R = R_1 + R_2 + R_3$$

Example

What single resistor could replace the three resistors shown in the diagram below?

1.4 kΩ   2.2 kΩ   3.7 kΩ
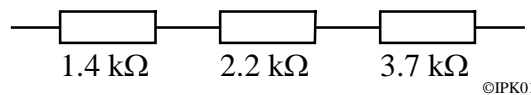
$$\Rightarrow R = R_1 + R_2 + R_3 = 1.4 + 2.2 + 3.7 = 7.1k\Omega$$

Resistors In Parallel

When two resistors, eg. R_1 and R_2, are connected in parallel, as in figure 3.6,

- the voltage across each resistor is the same, **V**,

- the total current, **I**, is equal to the sum of the currents in the separate resistors,

$$I = I_1 + I_2$$

- the resulting resistance, **R**, is given by:-

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2}$$
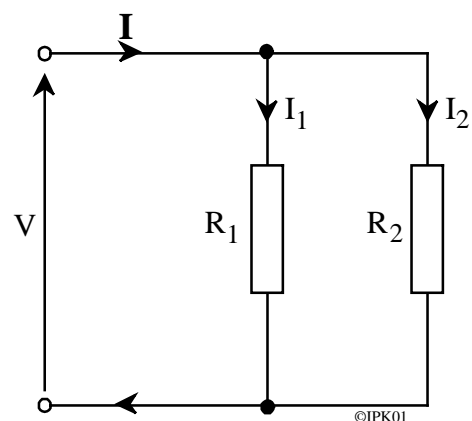
Figure 3.6.

Example

What single resistor could replace the two resistors shown in the diagram below?

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} = \frac{1}{10} + \frac{1}{5} = \frac{1+2}{10} = \frac{3}{10}$$

$$\Rightarrow R = \frac{10}{3} = 3.3k\Omega$$

10kΩ

5kΩ ©IPK01
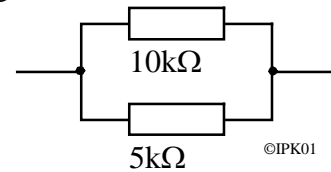
Since a resistor opposes the flow of electricity, it can be used to limit the current passing into a component. If a 6V, 60mA lamp was to be used in a circuit operating from 12V, too much current would pass through the lamp and it would be destroyed. If a suitable resistor is connected is series with the lamp, then the resistor can limit the current flowing to a safe level for the lamp. The arrangement is shown in figure 3.7.

lamp

12V

resistor

©IPK01
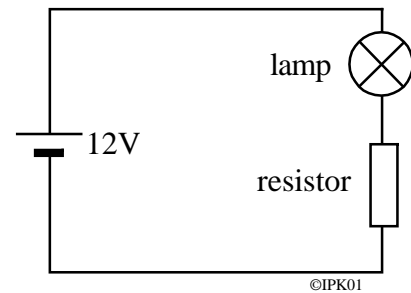
Figure 3.7

The value of the resistor is calculated using Ohm's law.

The current passing through the resistor is the same as through the lamp, i.e. 60mA. The lamp only requires 6V, and so there must be (12 – 6)V across the resistor, i.e. 6V. Using Ohm's law,

$$R = \frac{V}{I} = \frac{6}{0.06} = 100\Omega$$

Therefore the value of the resistor should be 100Ω.
This technique has many applications in electronics especially with LEDs and Zener diodes.

Heating And Magnetic Effects Of An Electric Current

When electrons pass through a material, they 'collide' with the atoms that make up the material. With each collision they lose a small amount of energy, which is transformed into heat within the material. So when a current passes through a material, the material is heated.

The amount of heat produced depends on the following:

the current flowing,
the resistance of the material.

Each electron has associated with it a very small magnetic field. When electrons are moving around randomly within a conductor the overall magnetic field created is zero because the random fields of each electron cancel. When electrons are forced to move in the same direction, i.e. when there is an electric current, then the magnetic field of each electron are no longer random and a net magnetic field is created. The strength of the magnetic field is determined by how many electrons are forced to pass in the same direction i.e. on the strength of the electric current.

So an electric current produces both a **heating effect** and a **magnetic effect**.

Electric Power

It can be shown quite simply that the electric power given out (dissipated) by a component is the product of the voltage across the component and the current through the component, i.e.

$$P = V \times I$$

But Ohm's law states that $\qquad V = I \times R$

Combining these formulae together gives two more equations for power

$$P = I^2 \times R \text{ and } P = \frac{V^2}{R}$$

eg.   A current of 0.5A passes through a component when there is 6V across it. What power is dissipated in the component?

$$P = V \times I = 6 \times 0.5 = 3W$$

eg.   A 60W lamp operates from a 230V supply. What is the resistance of the lamp?

$$P = \frac{V^2}{R}$$

$$\Rightarrow R = \frac{V^2}{P} = \frac{230^2}{60} = 882\Omega$$

Resistors

A resistor is a component that restricts the electric current passing through a circuit. It is therefore useful for limiting the amount of current passing through a component. A resistor is also useful for providing a voltage across it when a current is passed through it.

Resistors are either shaped like a tube with a wire coming from each end or as a tiny square with two solder connections, if it is a *surface mounted* resistor. Both types have the symbol shown in figure 3.8.
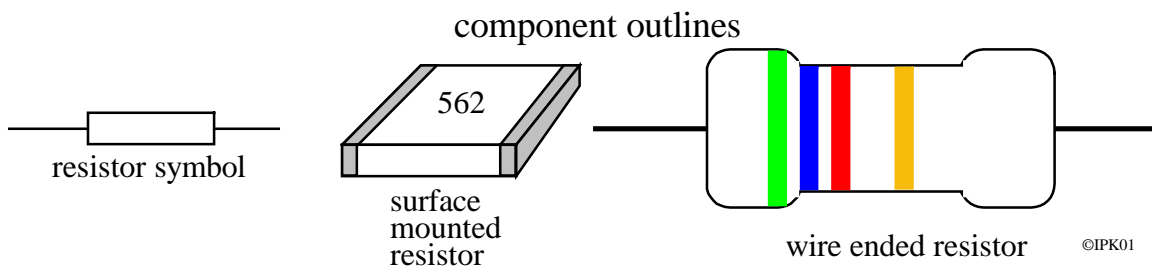
component outlines

resistor symbol

562

surface
mounted
resistor

wire ended resistor

©IPK01

Figure 3.8

insulation

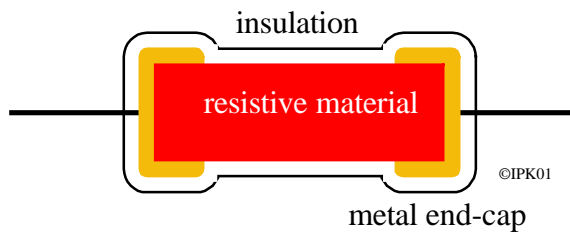resistive material

©IPK01

metal end-cap

Figure 3.9

A resistor consists of two metal end caps with a resistive material placed in between as shown in the cross-sectional diagram in figure 3.9.

There are three common substances used for the resistive material. These are Carbon, Metal Oxide and Thin Wire.

Carbon resistors are cheap but they tend to be unstable (their resistance changes with temperature and time) and can produce unwanted noise in circuits.

Metal oxide resistors are more expensive but are more accurate (smaller tolerance), more stable and produce much less electrical noise.

Wire wound resistors are the most expensive but can be very stable and accurate. They can often be designed to dissipate large amounts of power. However, because they are made from a coil of fine wire they are of little use in radio circuits since they have appreciable inductance.

Resistors are measured in units called **ohms**, in memory of Georg Simon Ohm who did much work on resistance during the nineteenth century. The symbol for the ohm is the capital Greek letter Omega drawn as **Ω.**

Resistor Tolerance

Although manufacturing techniques have improved significantly during the last few years, the value of a resistor is unlikely to be exactly the same as the value marked on it. The tolerance of a resistor shows how close its actual value was to its marked value when it was made.
eg a 100Ω resistor with a tolerance of ±10% could have a value between 90Ω (100 - 10) and 110Ω (100 + 10).

Typical tolerances are ±1%, ±2%, ±5% and ±10% and individual resistors are marked accordingly.

Printed Code

This code, BS1852, is printed on resistors, variable resistors and is also sometimes used on circuit diagrams. It consists of letters and numbers.

$$\mathbf{R \equiv \times 1 \quad K \equiv \times 1000 \quad M \equiv \times 1000000}$$

The position of the letter indicates the position of the decimal point,

eg.   4R7 ≡ 4.7 Ω,   4K7 ≡ 4.7 kΩ   4M7 ≡ 4.7 MΩ

The tolerance of the resistor is given by the letter at the end of the code.
The letters used are:-

$$\mathbf{F = ±1\%, \quad G = ± 2\%, \quad J = ± 5\%, \quad K = ± 10\%, \quad M = ± 20\%}$$

eg.   270RG = 270Ω ± 2% ,   47KJ = 47kΩ ± 5% ,   1M5K = 1.5MΩ ± 10%.

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Resistor Band Colour Coding

A resistor has either four or five coloured bands painted on it, as in figure 3.10.
The first two or three bands give
the value in significant figures,
the **next** gives the multiplier and
the **last** the tolerance.

©IPK01
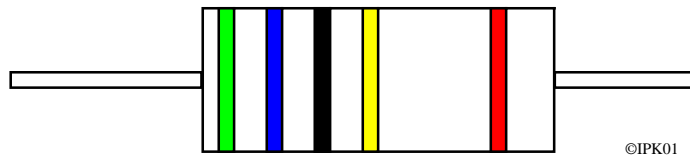
Figure 3.10.

Colour.	First	Second	Third	Next	Last
Black	0	0	0	—	—
Brown	1	1	1	0	±1%
Red	2	2	2	00	±2%
Orange	3	3	3	000	—
Yellow	4	4	4	0000	—
Green	5	5	5	00000	—
Blue	6	6	6	000000	—
Violet	7	7	7	—	—
Grey	8	8	8	—	—
White	9	9	9	—	—
Silver	—	—	—	0.01	±10%
Gold	—	—	—	0.1	±5%

NB.   Ignore the shaded column of the table for four band resistors

eg.   a 5 band resistor with bands of green, blue, black, yellow, red
        has a value of   5 - 6 - 0 - 0000 - ±2%
                          i.e. $5.6M\Omega \pm 2\%$.

eg.   a 4 band resistor with bands of yellow, violet, brown and gold
        has a value of   4 - 7 - 0 - ±5%
                          i.e. $470\Omega \pm 5\%$.

Preferred Values

Since exact values of fixed resistors are unnecessary in most circuits, only certain *preferred* values are made. The values chosen for the E24 series (with ± 5% tolerance) are as follows.

1.0, 1.1, 1.2, 1.3, 1.5, 1.6, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.6, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1, and multiples that are powers of ten greater.

These values give maximum coverage with minimum overlap with the ± 5% tolerance.

When a resistor value has been calculated it will often fall in between two of the preferred values. The one that is chosen will depend on the application within the circuit. If the absolute maximum value for current flow has been used in the calculation then it will usually mean that the preferred value that is the next largest to the calculated value will be selected. This will

ensure that the maximum current is not exceeded. This is an important consideration when working with LEDs and Zener diodes.

10.4 DIODES

Light Emitting Diode (LED)

LEDs provide a very convenient way of obtaining an output from the processor of an electronic system, since they can be interfaced directly to logic gates.
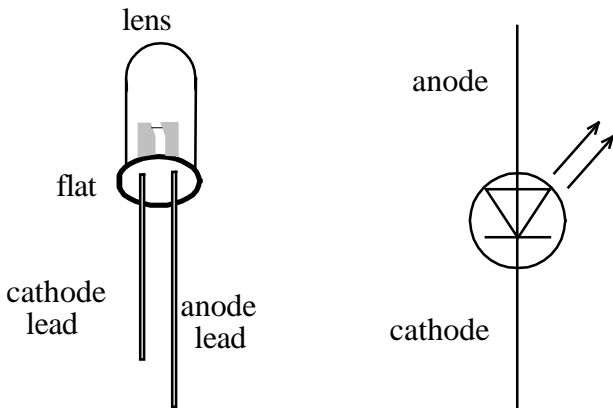
An LED is a diode made from the semi-conductor gallium arsenide phosphide. Its component outline and symbol are shown in figure 4.1. When forward biased (see next section on diodes) it conducts and emits light of a certain colour depending on its composition. No light emission occurs in reverse bias and if the reverse voltage exceeds approximately 5V then the LED may be damaged.

Figure 4.1

©IPK01

A LED requires a series resistor to ensure the current does not exceed its maximum rating, which should be taken as 20mA. The forward voltage drop across a LED is about 1.8V, though it does depend upon the colour of the LED.

To calculate the value of the series resistor it is first necessary to decide on the current that should flow through the LED. The data sheet for the LED will specify a maximum current, I_{max}. The LED current should be less than this. If the supply voltage is V_s, then

$$R = \frac{V_s - 1.8}{I_{max}}$$

Figure 4.2   ©IPK01

The **minimum** value used for R should be the next **largest** preferred value.

LEDs are used as indicator lamps and in seven-segment displays. They have the advantages of small size, long life, a small operating current and high operating speed. There is now a large range of different LEDs readily available with outputs ranging from the infra-red to the blue wavelengths and sizes ranging from 1mm to 50mm.

Seven segment array

Electronic calculators, clocks, cash registers and measuring instruments often have seven-segment LED displays as numerical indicators. Each segment is an LED and by lighting up different segments all numbers from 0 to 9 can be displayed. Each segment needs a separate current limiting resistor to prevent damage to the segment by excess power dissipation.
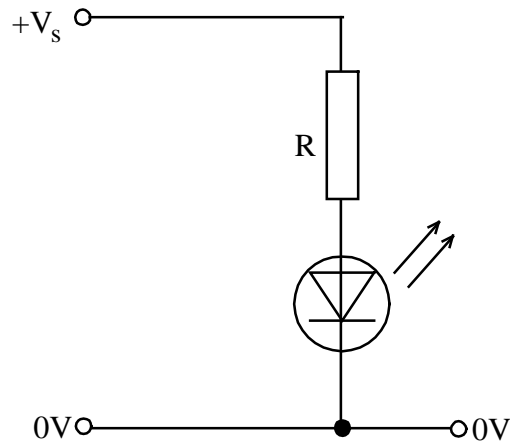
All the cathodes (common cathode type) or all the anodes (common anode type) are joined to form a common connection.
(If the driving circuit is made from transistors, so that the seven-segment display segments are connected in the collector circuits, then a common anode display will be required.)
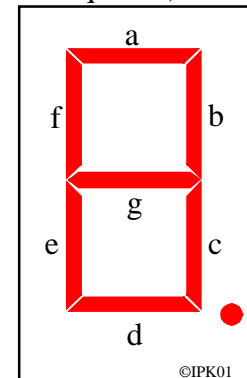
Diodes

A diode is a semiconductor device that only allows current to pass one way. The symbol for a diode is shown in figure 4.4, the direction of the arrow indicating the direction of the conventional current flow from anode to cathode.

Figure 4.3

anode —▷|— cathode

symbol

anode ——[|]—— cathode

component outline
Figure 4.4
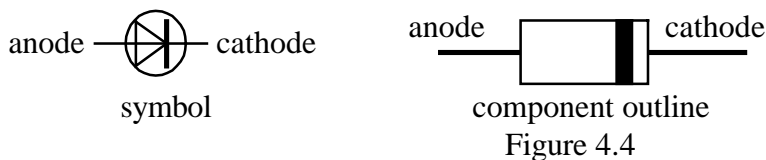
When the current passes from the anode to the cathode of the diode, the anode is positive with respect to the cathode and the diode is said to be *forward biased.*
When the cathode of a diode is positive with respect to the anode then no current will flow and the diode is said to be *reverse biased.*

When a silicon diode is forward biased, conduction does not start until the voltage across it is about 0.7V. Once conduction has started, a very small increase in voltage produces a large increase in the current as shown in the diode characteristics in figure 4.5. (Figure 4.5(b) is an enlarged version of the forward biased section of figure 4.5(a).)

Figure 4.5(a)

Figure 4.5(b)

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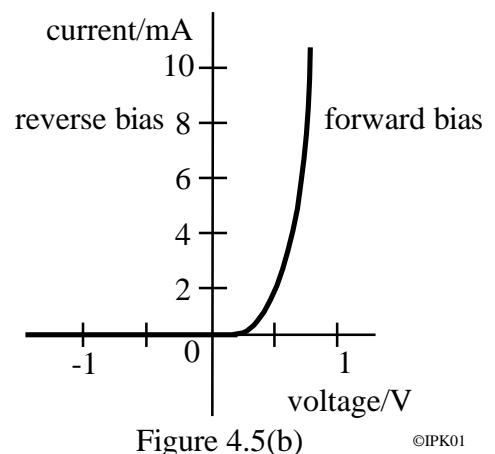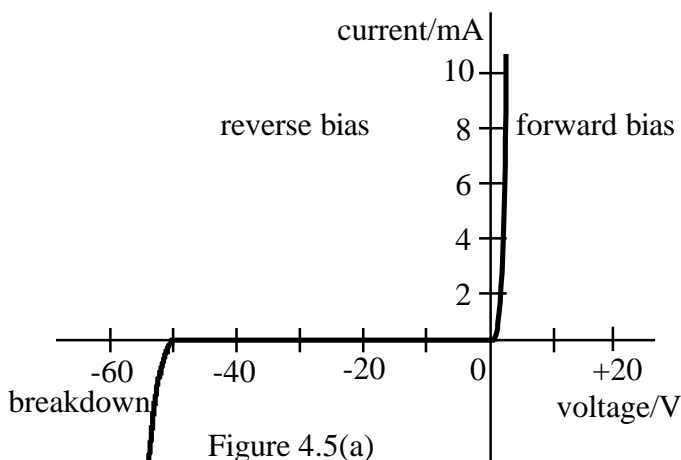
Using Diodes To Extend The Number Of Inputs On A Logic Gate

Diodes can be used to successfully increase the number of inputs on a logic gate so long as the circuit is not operating at a high frequency (less than 10kHz) and the high input impedance of a normal logic gate can be sacrificed. The noise immunity of the circuit will also be degraded, though the extent of the degradation will depend on the supply voltage being used with the logic gates.

The circuits shown below are based on a NOT gate but the same principle can be applied to the input of any other logic gate. It is assumed that the logic gate belongs to one of the CMOS families.

Many Input NOR Gate

In the absence of any inputs, the 100kΩ resistor ensures that the input of the NOT gate is at logic 0, (it is acting as a *pull-down* resistor). The output of the NOT gate is therefore logic 1 and any logic 0 inputs will not alter the output. But any logic 1 inputs will forward bias the diode and make the NOT gate input a logic 1. The output of the NOT gate will become logic 0.
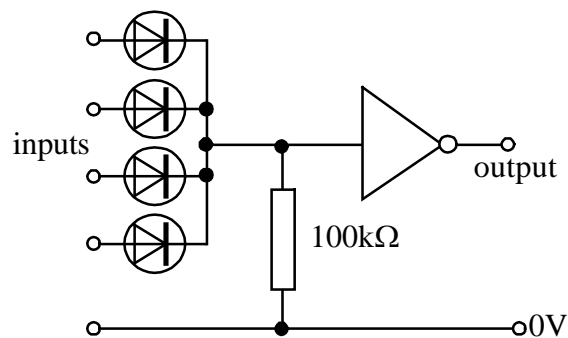
Figure 4.6   ©IPK01

Many Input NAND Gate

In the absence of any inputs, the 100kΩ resistor ensures that the input of the NOT gate is at logic 1, (it is acting as a *pull-up* resistor). The output of the NOT gate is therefore logic 0 and any logic 1 inputs will not alter the output. But any logic 0 inputs will forward bias the diode and make the NOT gate input a logic 0. The output of the NOT gate will become logic 1. Therefore, the NOT gate output will only be logic 0 when all of the inputs are logic 1.
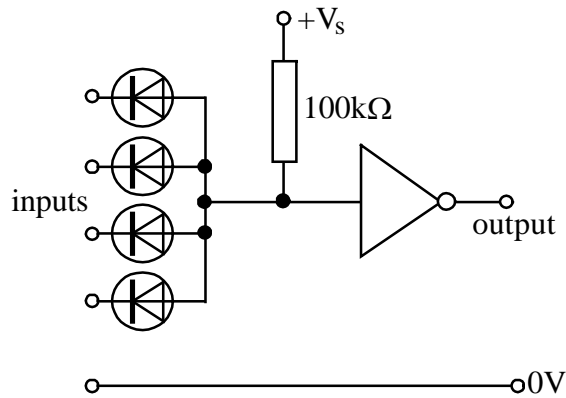
Figure 4.7   ©IPK01

Although the examples in figures 4.6 and 4.7 show four input gates being formed, the technique can be expanded to as many or as few inputs as required. It can also be used on the individual inputs of NAND and NOR gates.
In the examples above, the input impedance of the circuits is that of the pull-up or pull-down resistor. This resistor can be any value in the range from 10kΩ to 10MΩ, though very high resistor values should only be used with low frequency circuits.

Zener diodes

Logic gates, along with many other electronic circuits, behave more predictably when they are operated from a stabilised power supply. Zener diodes provide a cheap and convenient method of providing a stabilised supply.

If the peak inverse voltage of a normal diode is exceeded the diode is usually damaged. A zener diode is designed so that at a certain breakdown voltage the reverse current increases suddenly, as shown by the characteristic in figure 4.8. At this breakdown voltage the reverse current is limited by a series resistor so the voltage across the zener diode, V_Z, remains constant over a wide range of reverse currents passing through the zener diode.
Zener diodes are made with breakdown voltages between 2.7V and 200V.
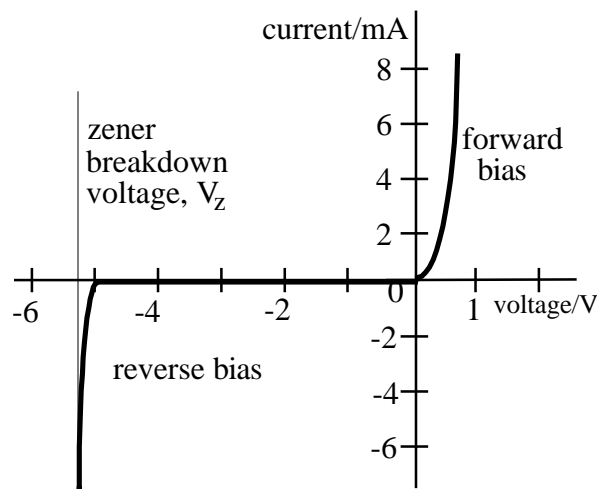
Figure 4.8   ©IPK01

As well as providing voltage regulation to obtain a steady voltage in circuits where the supply voltage varies, a zener diode can also be used to:-

a).   prevent the voltage difference in a system exceeding a chosen value,

b).   reduce a voltage by a certain amount, irrespective of the current flowing.

In an unregulated power supply the output voltage falls when the output current rises. A zener diode can be used to minimise this effect using the circuit shown in figure 4.9.

Figure 4.9

To calculate the minimum value of the current limiting resistor, R, it is necessary to know the following:

the maximum input voltage V_{max},

the maximum power dissipation of the zener diode, P_{max},

the minimum current needed to flow through the zener diode, I_{min}.

The maximum current that can flow through the zener

diode, I_z, is determined by the power rating of the diode.

$$I_z = \frac{P_{max}}{V_z}$$

Therefore the maximum current that can be used by the load while the output voltage is kept constant is

$$I_{load} = I_z - I_{min}.$$

The minimum value of the current limiting resistor, R, is calculated using the formula

$$R = \frac{V_{max} - V_z}{I_z}.$$

If the load current rises (or falls) the zener current falls (or rises) by the same amount. This is because the zener tries to maintain a constant voltage across itself. If the load current becomes greater than I_z, then the voltage across the zener diode will decrease.

If the output is short circuited, then the maximum current that can flow is $\dfrac{V_{max}}{R}$.

Under normal operating conditions the resistor R has to dissipate a power equal to

$$I_z \times (V_{max} - V_z)$$

When the output is short-circuited the resistor R has to dissipate a power equal to $I_z \times V_{max}$

Example

A stabilised 5.1V power supply is required to operate a logic circuit in an electronic system. The system is to be operated from a 9V battery. A 5.1V, 400mW zener diode is available, which requires a minimum current of 2mA to maintain the zener voltage.

The required circuit diagram is shown in figure 4.10 below. It is the same as figure 4.9 except that an output capacitor (100nF) has been added to remove noise from the zener diode.
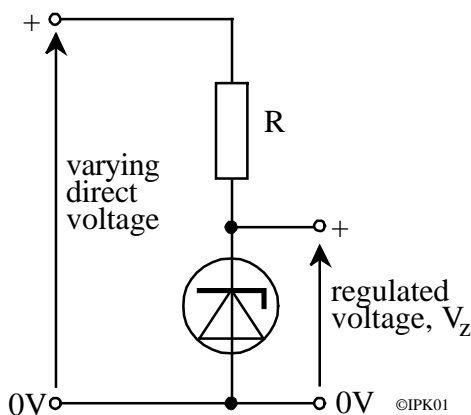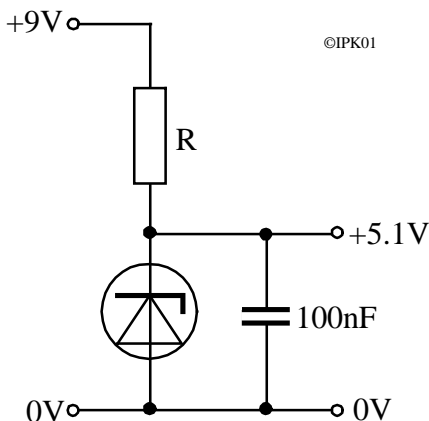

Figure 4.10

The maximum current that should pass through the zener diode is 0.4/5.1 = 78.4mA.
The voltage across the resistor is 9 – 5.1 = 3.9V.
Therefore the value of the resistor = 3.9/0.0784 = 49.7Ω
In order not to damage the zener diode, the nearest greater preferred value is chosen i.e. a resistor of 51Ω should be used.

The power dissipated by the resistor = $3.9^2/51 = 0.298$W.
Therefore a 0.5W resistor should be used.

If the logic circuit only needs a few mA then there is no point in allowing a large current to pass through the zener diode as it will just discharge the battery. It would be a useful exercise to verify that a suitable resistor, if the logic circuit only required 10mA, would be 300Ω.

10.5   RESISTIVE INPUT TRANSDUCERS

In order for electronic systems to be useful, they must be able to respond to different input parameters. Resistive input transducers in the form of Light Dependent Resistors and Thermistors enable variations in light intensity and temperature to be converted into electrical signals for electronic systems.

The Light Dependent Resistor (LDR)

The resistance of a light dependent resistor decreases as the illumination on it increases. It can therefore convert changes in light intensity into changes in electric current. The LDR consists of metal electrodes embedded into the surface of a film of cadmium sulphide. Its component outline, symbol and a typical characteristic are shown in figure 5.1.
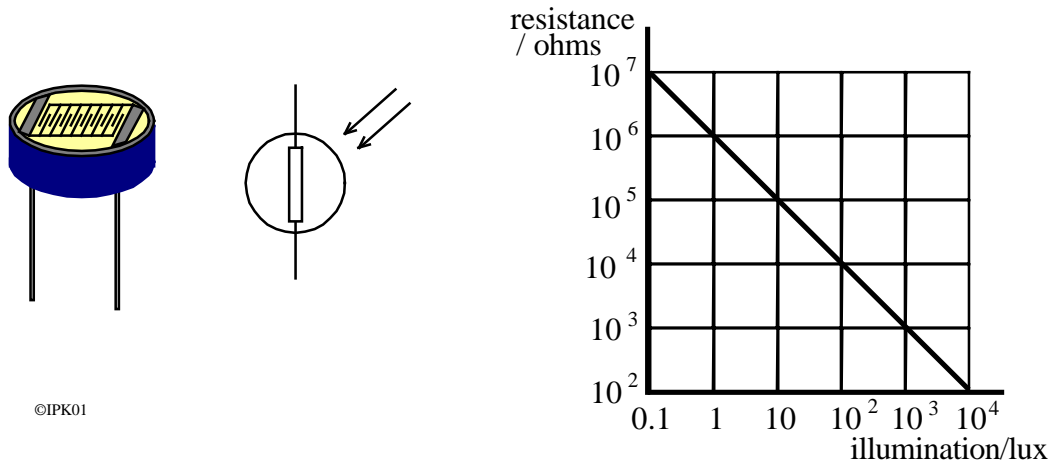
Figure 5.1

There is only one type of LDR readily available and it has the code number of ORP12.

Thermistors (negative temperature coefficient, n.t.c.)

This is a resistor whose resistance decreases considerably when its temperature rises.
It can therefore convert changes in temperature into changes in electric current. Its component outline, symbol and a typical characteristic are shown in figure 5.2.
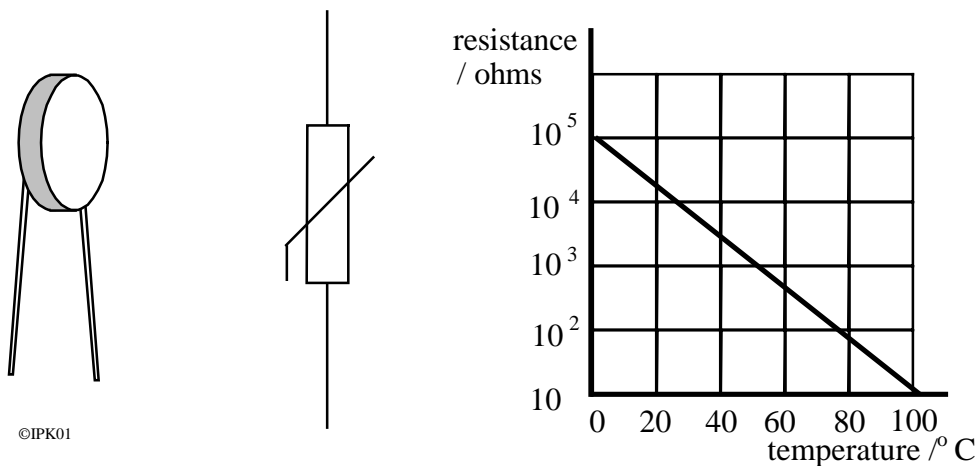
Figure 5.2

There is a very large number of different types of thermistor available varying in both physical size and the change of resistance with temperature.

Neither of these devices, when used on their own, will produce an electrical signal. Since it is their resistance that varies, and most electronic systems need a variation in voltage as an input, it is necessary to incorporate these sensors into a circuit which will change a variation in resistance into a voltage change. The circuit usually used for this purpose is the Voltage Divider.

Voltage Dividers

Two fixed resistors can be used to obtain a lower voltage from a fixed voltage supply. The circuit diagram of a voltage divider is shown in figure 5.3. The voltage across each resistor is in the same ratio as their resistances and so in many applications the output voltage can be determined by simple proportion. However, it is worth considering how to calculate the output voltage.

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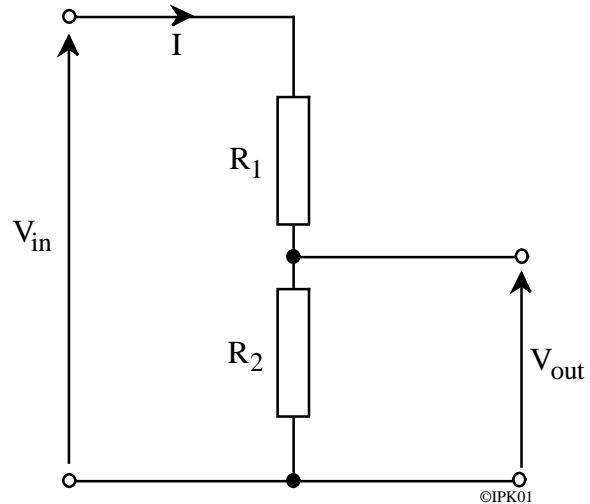
Figure 5.3

Resistors R_1 and R_2 are connected in series across V_{in}. Assuming that no current is passing from the output then a current, I, will pass through these resistors where

$$I = \frac{V_{in}}{R_1 + R_2}$$

The output voltage, V_{out} , is now given by

$$V_{out} = I \times R_2 = \frac{V_{in} \times R_2}{R_1 + R_2}$$

So

$$V_{out} = \frac{V_{in} \times R_2}{R_1 + R_2}$$

Although this formula is only valid if there is no current passing from the output of the voltage divider, in many applications an output current of I/20 will not produce a significant error.

Example

The output voltage from a CD player is 0.5V and an amplifier only requires an input signal of 0.05V to give maximum power. The CD player needs to operate into a resistance of at least 47kΩ. Design a suitable voltage divider to enable the CD player to be connected to the amplifier.

Problems of this type often cause difficulties because the circuit designer has to make a decision as to one of the component values. In this case the information about the CD player

is helpful and since the minimum resistance for the CD player is 47kΩ, R_2 can be set at this value. The voltage divider formula needs rearranging so that R_1 can be found with the formula below.

$$R_1 = \frac{V_{in} \times R_2}{V_{out}} - R_2$$

The values can now be substituted and R_1 calculated.

$$R_1 = \frac{0.5 \times 47}{0.05} - 47 = 423k\Omega$$

The nearest preferred value to this is **430kΩ**.

Using Resistive Input Transducers With A Voltage Divider

Consider the circuit in figure 5.4. Resistor R_1 has been replaced with a LDR which has a resistance of 1MΩ in the dark and 100Ω in bright light.
It is a worthwhile exercise to verify that in the dark, V_{out} is 0.089V and in the light, V_{out} is 8.9V.
This circuit, therefore, gives a logic 0 output in the dark and a logic 1 output in the light.
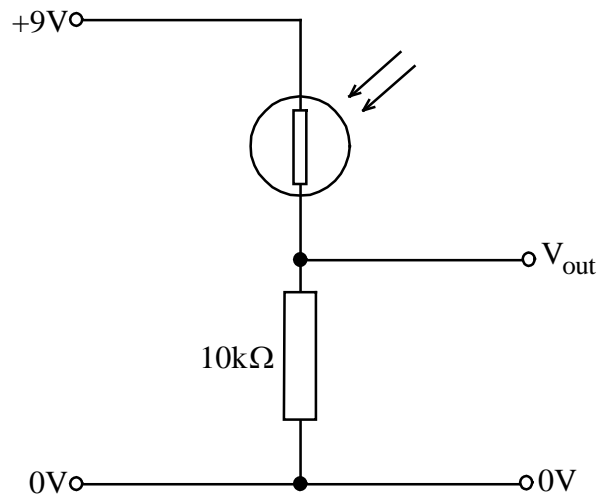
Figure 5.4

©IPK01
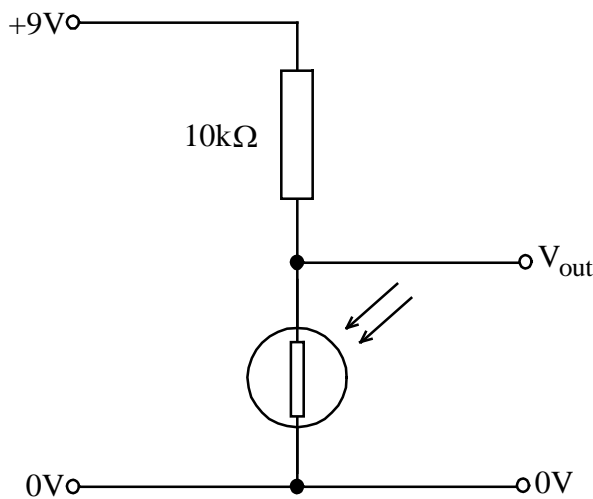
Figure 5.5

©IPK01

Consider the circuit in figure 5.5. Resistor R_2 has been replaced with a LDR which has a resistance of 1MΩ in the dark and 100Ω in bright light.
It is a worthwhile exercise to verify that in the dark, V_{out} is 8.9V and in the light, V_{out} is 0.089V.
This circuit, therefore, gives a logic 1 output in the dark and a logic 0 output in the light.

In both of these circuits the LDR could be replaced with a thermistor, so that the output voltage was dependent upon temperature rather than on light intensity.

These circuits can be connected directly to CMOS type logic gates, since the gates have a very high input resistance and take almost no current from the output of the potential divider.

Although the output from a voltage divider can be connected directly to a logic gate, the output from the voltage divider itself is analogue and not digital. Considering the circuit in figure 5.4, the output can have any value from 0.089V to 8.9V depending upon the light level. The transfer characteristic of a logic gate (graph of output voltage as a function of input voltage) will therefore determine the range of light levels that the logic gate considers to be a logic 0 input and what it considers to be a logic 1 input.

All module test questions will assume that the input switching voltage is at half of the supply voltage, but in practical circuits this may well be different.

The graphs in figure 5.6 below show the transfer characteristics for a two input CMOS NAND gate (CD4011BCN) operating with a supply of 5V and 9V respectively. The test circuits are shown by the side for reference.
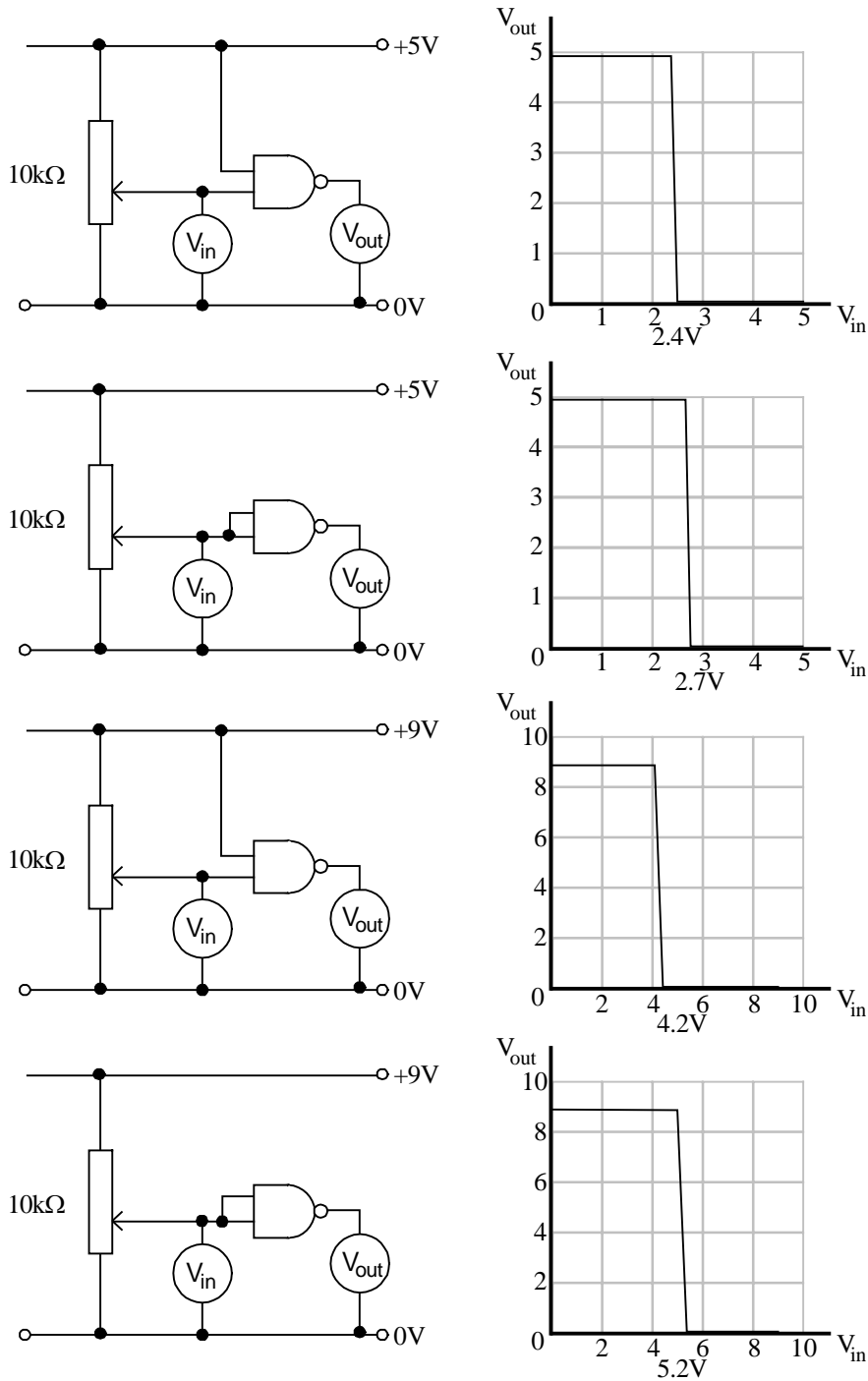
Figure 5.6

Example

Consider the circuit diagram in figure 5.7. Assuming that the logic gate switches at an input of 4.5V and that the LDR has the characteristic curve shown in figure 5.1, verify that the output will change state at a light level of 100 lux, and that the output will be logic 0 at a light level of 200 lux.
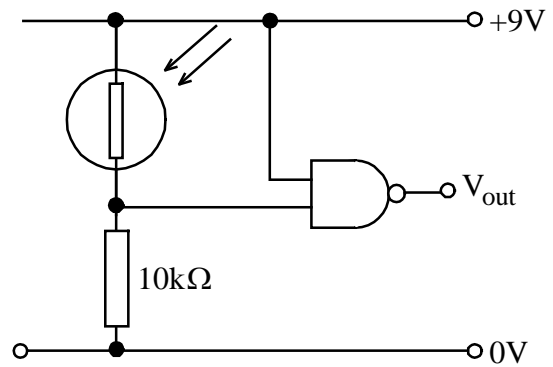
Figure 5.7   ©IPK01

Variable Resistors (Potentiometers)

A variable resistor is a convenient means of changing a resistor value. It consists of a track of fixed resistance and a wiper that moves over the track. There are two main types, rotary and linear variable resistors as shown in figure 5.8.
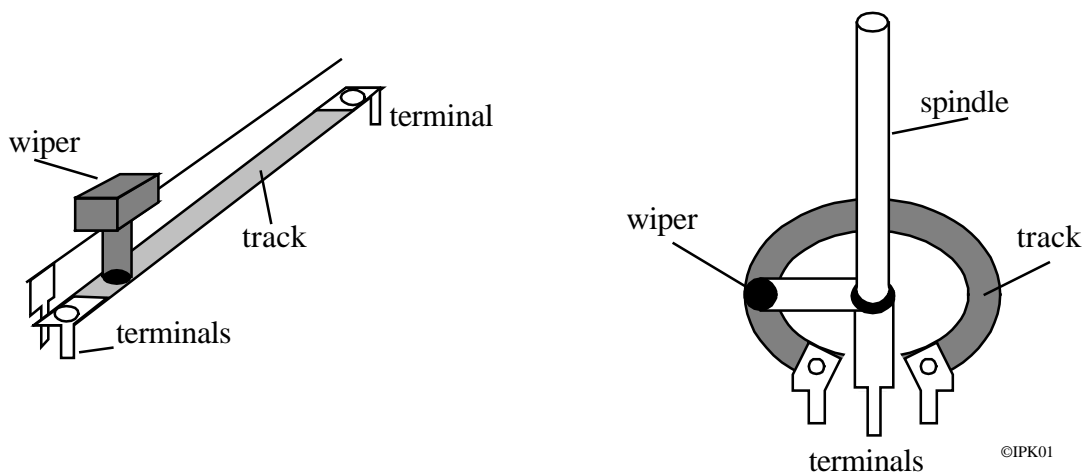
Figure 5.8

Both types of variable resistor are available with **Linear** or **Logarithmic** tracks. The logarithmic track variable resistors are predominantly used as volume controls on audio systems since its adjustment matches the change in volume as perceived by the ear.

Both types of variable resistor can be used directly as voltage dividers by connecting the ends of the track across the power-supply, and taking the output from the wiper terminal and one of the end of track terminals (as in figure 5.6). Since the output voltage will depend on the position of the wiper, they can be used as position sensors for electronic systems.

10.6   TRANSISTORS AND MOSFETS

Logic gates are only able to supply enough current (a few mA) to operate LEDs as output devices. In order to operate more powerful output devices it is necessary to interface the logic gate to the output device by a '**driver**' or '**power switch**'. Two of the most important drivers are junction transistors and MOSFETs. These devices are able to switch currents of up to 100A and voltages up to 1000V.

A junction transistor is a three terminal semiconductor device that is able to provide current amplification. There are two types of junction transistor, those which amplify a positive current, which are known as **npn transistors** and those which amplify a negative current, which are known as **pnp transistors**. Their symbols and current flow diagrams are shown in figure 6.1
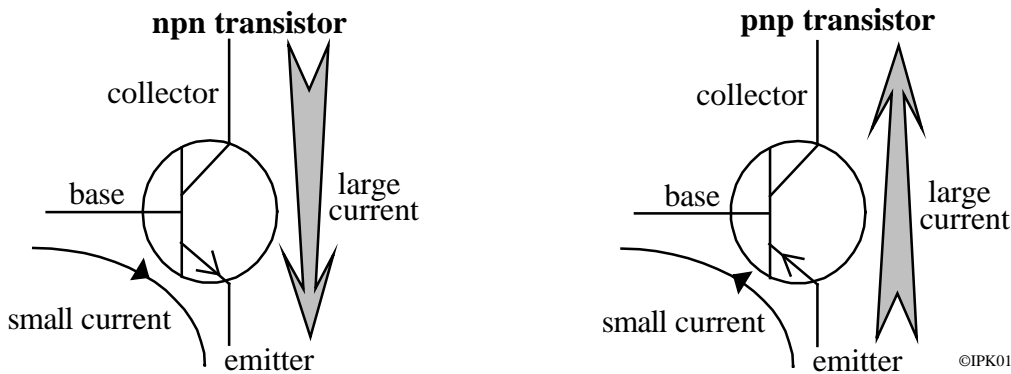
Figure 6.1

Only a knowledge of npn transistors is required for this module specification.

Transistors come in several shapes and sizes as shown in figure 6.2.
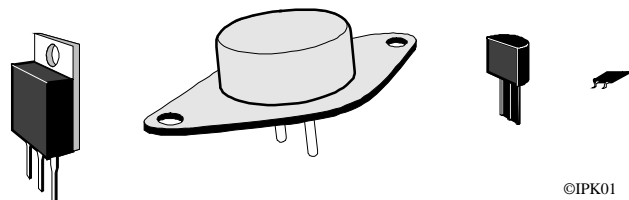
Figure 6.2

In normal operation, the base-emitter junction of a transistor behaves like a forward biased diode. When a small current passes through the base emitter junction a much larger current is made to pass through the collect and emitter. Since the base emitter behaves as a forward biased diode, for a silicon transistor there will be a voltage of 0.7V between the base and emitter when a collector current passes.

Figure 6.3 shows an npn transistor arranged as a switch and the variation of V_{out} with V_{in}.
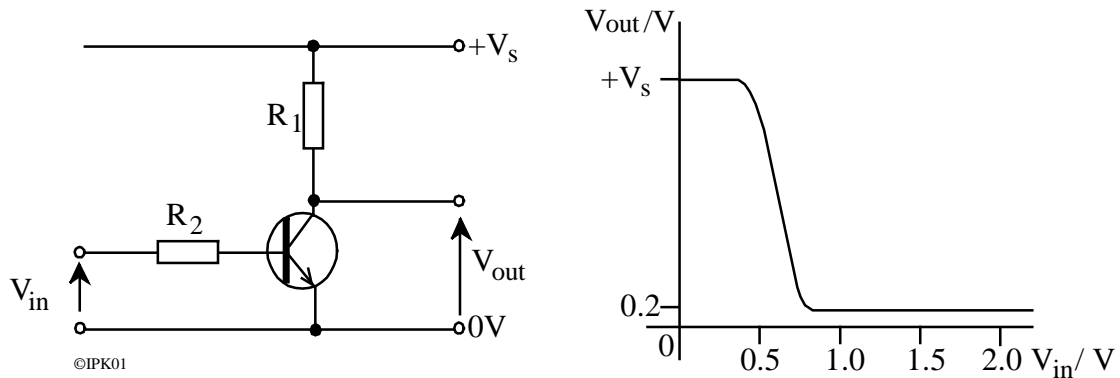
Figure 6.3

As can be seen from the graph of V_{out} against V_{in}, the output voltage remains at the supply voltage, $+V_s$, until V_{in} approaches 0.5V. At this voltage a small collector current flows and V_{out} begins to fall. When V_{in} reaches about 0.7V, the maximum collector current is flowing (limited by R_1) and the transistor saturates with a collector-emitter voltage of about 0.2V. Any further increase in V_{in} has no effect on V_{out}. The transistor is therefore operating as a switch.

When V_{in} is less than 0.5V, V_{out} is equal to the supply voltage.
When V_{in} is greater than 0.7V, V_{out} is 0.2V.

The resistor in the collector circuit, R_1, can be replaced with any form of load, eg. a 12V, 6W lamp that needs to be switched by a small current, eg. from a logic gate, as in figure 6.4.

Figure 6.4

There are many different transistors available and the one selected should be able to:

operate at the supply voltage (V_{ce})
pass sufficient collector current (I_c)
dissipate sufficient power (P_{tot})
give a large current gain (h_{FE})
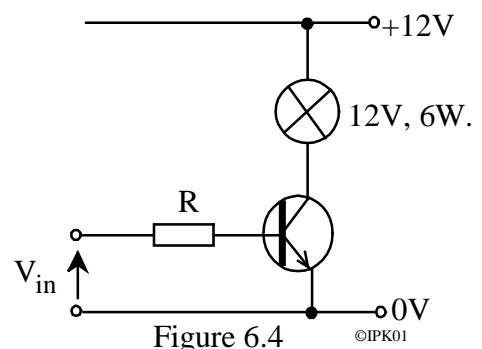
For this example, its V_{ce} (voltage across the collector and emitter) must be greater than 12V.

For a 6W lamp operating on 12V, the current is 0.5A, so its I_c (collector current) must be greater than 0.5A.

When the transistor is switched on, there is approximately 0.2V across the collector and emitter. The current passing is 0.5A and so the power dissipated by the transistor is $0.2 \times 0.5 = 0.1W$. Its P_{tot} must, therefore, be greater than 0.1W.

Its h_{FE} is a measure of how many times larger the collector current is than the base current. If possible, a transistor should be chosen so that h_{FE} is greater than 100 at the required collector current.

Using components that are operating at the limit of their specification leads to poor reliability. A suitable transistor for carrying out the switching function in figure 6.4 would be a ZTX851, and it is a useful exercise to verify the specifications using a component catalogue.

In selecting a suitable value for the resistor in series with the base of the transistor, sufficient base current needs to pass so that the transistor passes as much as possible, ie it is saturated. However, the resistor needs to prevent too much current from passing so that the base-emitter junction of the transistor is damaged. As a general rule, a current of up to 10mA can pass into the base of a small junction transistor. Assuming that the output voltage from the logic gate operating the transistor is 5V, and taking account of the 0.7V across the base-emitter junction of the transistor, the voltage across R is equal to

$$5 - 0.7 = 4.3V$$

Allowing a maximum base current of 10mA, the value of R can be found from Ohm's law,

$$R = \frac{4.3}{0.01} = 430\Omega$$

A suitable base resistor in this application would therefore be **470Ω**

The input resistance of a transistor switch circuit is low, ie of the order of 1kΩ. This can provide an unacceptable current drain on some logic circuits. A better alternative to junction transistors are enhancement mode MOSFETs.

Enhancement Mode MOSFETs

Enhancement mode MOSFETS are voltage operated, three terminal semiconductor devices. They have a very large input resistance, (>50MΩ), and a correspondingly large current gain. Their electrical symbols and current flows are shown in figure 6.25.

n-channel MOSFET   p-channel MOSFET
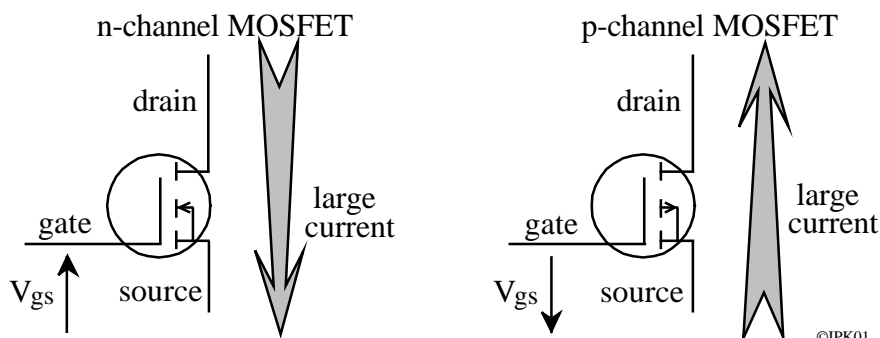
Figure 6.5

This syllabus only requires a knowledge of the n-channel MOSFET.
To obtain a drain current, I_d, a voltage, V_{gs}, is applied between the gate and source.

Figure 6.6 shows an n-channel MOSFET arranged as a switch.
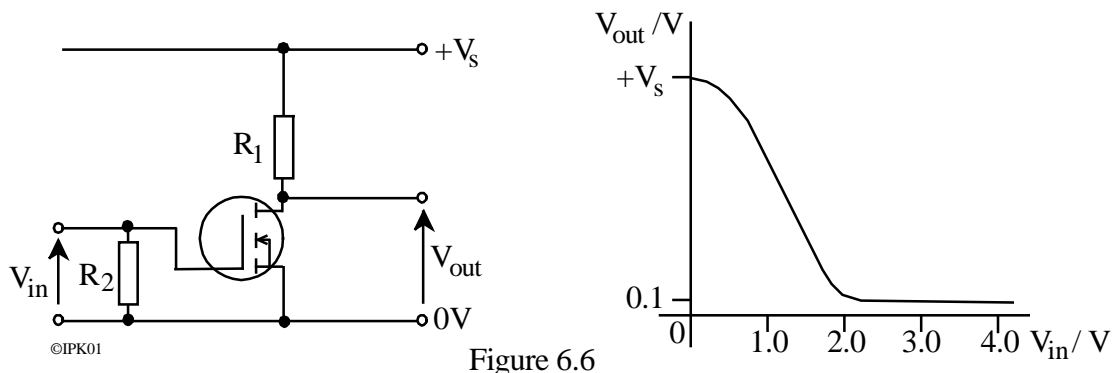
Figure 6.6

As can be seen from the graph of V_{out} against V_{in}, the output voltage starts to fall as soon as V_{gs} is greater than 0V. Drain current passes and the MOSFET saturates at about 0.1V, when V_{gs} is about 2V. (The actual saturation voltage depends upon the drain current passing.) Any further increase in V_{in} has no effect on V_{out}. The MOSFET is therefore operating as a switch in the same way as the transistor.

It is a useful exercise to consider the circuit in figure 6.4, but with the transistor replaced by a MOSFET as in figure 6.7.

Again, there are many different MOSFETs available and the one selected should be able to:
- operate at the supply voltage (V_{DS}),
- pass sufficient drain current (I_D),
- dissipate sufficient power (P_D),
- give a very low drain to source resistance (R_{DS}).

For this example, V_{DS} (voltage across the drain and source) must be greater than 12V.

I_D (the drain current) must be greater than 0.5A.

R_{DS} (the drain to source resistance) must be low, preferably less than 0.1Ω.

With a value of $R_{DS} = 0.1Ω$, the power dissipated is

Figure 6.7   ©IPK01

$$\mathbf{P_D = I_D^2 \times R_{DS} = 0.5^2 \times 0.1 = 0.025W}$$

The resistor R_2 is not strictly necessary but it will prevent any damage to the MOSFET by static electricity. A typical value for R_2 would be 1MΩ.

Again, using components that are operating at the limit of their specification leads to poor reliability. A suitable MOSFET for carrying out the switching function in figure 6.7 would be a BUZ11 and it is a useful exercise to verify that the specification well exceeds the requirements in this application, though the device is relatively inexpensive.

The main advantages of a MOSFET over a junction transistor are:
- the very large input resistance, (although its impedance at high frequencies can be very low),
- the very large current gain,
- it has a positive thermal coefficient, ie if its temperature increases, the resistance from drain to source increases and so decreases the drain current flowing.

The main disadvantage of MOSFETs is that they are currently more expensive than junction transistors.
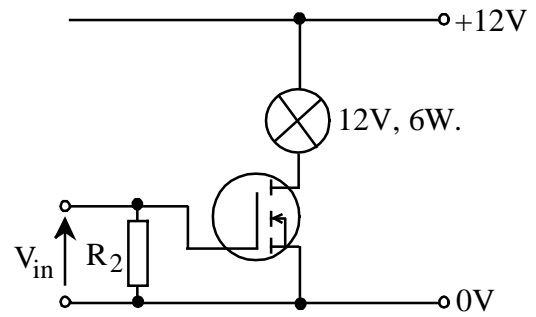
10.7   OUTPUT DEVICES

By using transistors and MOSFETs as drivers for logic gates, it is now possible to use electronic systems to control high power output devices. Some common high power output devices are described in this section, starting with the electromagnetic relay, which itself can be used as a driver for high power output devices.

Electromagnetic Relay

The basic structure is shown in figure 7.1.
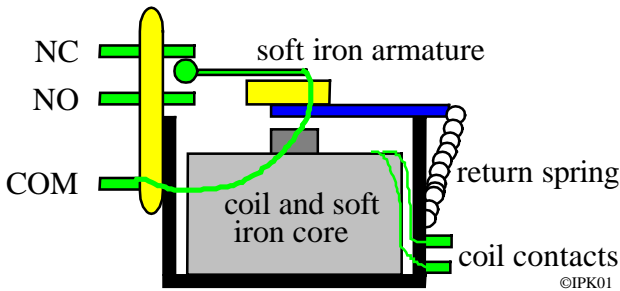
Figure 7.1

When a current flows in the circuit connected to the coil, the soft iron core is magnetised and attracts the soft iron armature. This rocks on a pivot and so closes the Normally Open (NO) contacts and opens the Normally Closed (NC) contacts. These contacts can be used to switch a separate circuit.

The current needed to operate a relay is called the **pull-in** current. The relay will switch back to its initial state when the current in the coil is reduced to a certain value, known as the **drop-out** current. A relay tends to be slow acting due to the mechanical movement of the armature.
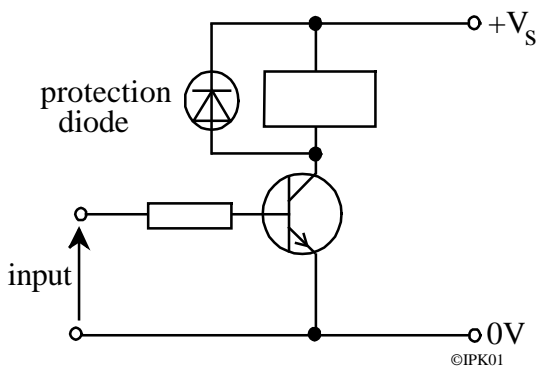
Figure 7.2

When the current in the coil of a relay falls to zero, i.e. when the transistor is switched off, a large voltage is induced in the coil due to its inductance. This induced voltage will damage the transistor being used to drive the relay. A diode is connected in parallel with the relay so that it is in reverse bias with the voltage supply. The diode offers an easy path to the induced voltage and so prevents it damaging the transistor, as in figure 7.2.

Electromagnetic Solenoids

In order for an electronic circuit to control a mechanical device, invariably some form of electromagnetic device is used. An electromagnetic solenoid essentially consists of a coil of wire and a soft iron armature, as shown in figure 7.3.

When the solenoid coil is energised, a magnetic field is produced at the centre of the coil and the soft iron armature is pulled into the centre of the coil, compressing the spring. When the coil is de-energised, the magnetic field collapses and the return spring pushes the armature back out of the coil.
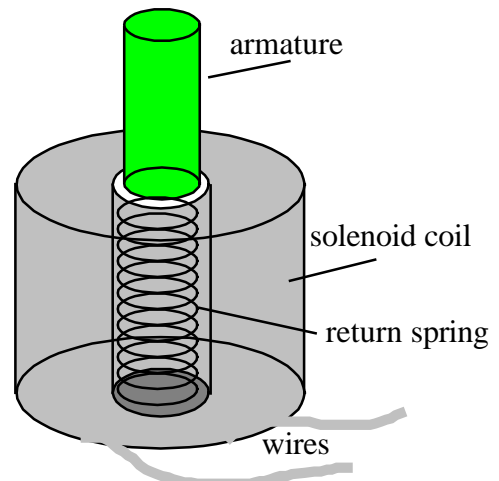
Figure 7.3

By attaching different mechanical systems to the armature, solenoids can be used to provide a wide variety of electromechanical devices ranging from door locks and mechanical counters to pneumatic and hydraulic control valves.

As far as the electronic drive circuitry is concerned, the current to be switched is determined from the operating voltage and the resistance of the coil. However, when the coil is de-energised, a substantial voltage is produced and so the driving semiconductor device **must** be protected by a diode, as for a relay.

Buzzers

A 'Buzzer' is a generic term for a device that can be used as an Audible Warning Device (AWD). When electricity is supplied to one of these devices, it produces an audible noise. There is a very wide variety of AWDs available ranging from the type that are used in digital watches to those that can be heard above the noise level of a large industrial factory!

There are two main types of AWDs, electro mechanical devices and piezo electric devices. An electromechanical buzzer consists of system which allows the electric current to be rapidly switched on off, so allowing a moving object to vibrate at an audible frequency. The classic electromechanical buzzer is the electric bell, where the current in an electromagnet is rapidly switched on and off. When the current flows, the electromagnet attracts an armature which in turn hits the gong of the bell. Such devices usually need a current in excess of 0.5A and the semiconductor driver will need protecting from the large voltage produced when the electromagnet is de-energised.
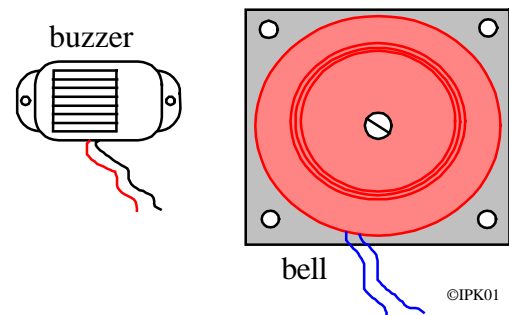
Another form of electromechanical buzzer consists of a small electronic circuit that repeatedly switches the current on and off to an electromagnet which attracts a thin metal plate. As the metal plate is attracted and then released it moves the air around it so creating a noise. These devices usually operate from 6 to 12V with a current of approximately 30mA. The semiconductor driver for these devices does not need protecting from large voltages as this is taken care of inside the buzzer itself.

Piezo electric devices are tiny plates of quartz crystal. When an electric field is applied to the crystal it flexes, returning to its original shape when the field is removed. If an electric field is continuously applied and removed at a frequency in the audible range, the crystal will vibrate and disturb the surrounding air, creating an audible noise. The amount the crystal flexes is normally very small and so to maximise the output sound, a frequency of 2.5 - 3kHz is used, this being the range of frequencies to which the ear is most sensitive. These devices operate from 3 to 12V and need a current of a few milliamps. As such they can often be connected directly to the output of a logic gate without needing any transistor or MOSFET driver.
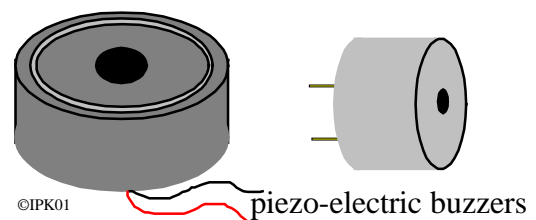
Motors

There are two common types of direct current (dc) motors, those with carbon brushes and a commutator, and those without. The motors without brushes, which include stepper motors, need an electronic control circuit to make them rotate. Such motors and the necessary electronic control systems are considered in A2, Module 3.

A motor with brushes, consists of a strong magnetic field in which an armature, containing an electromagnet rotates when an electric current is applied to it. An essential part of a dc motor is a mechanical switch which reverses the direction of the current flowing through the armature coils and so ensures its continuous rotation. Because the current is being switched to the armature coils, it is necessary for the semiconductor driving the motor to be protected, by means of a diode, from the large voltages produced when the current switches off.

The current required by a motor depends upon the resistance of the coils and the speed of rotation of the coils. When electric power is first supplied to a stationary motor, the current passing can be calculated by applying Ohm's law to the supply voltage and the resistance of the coils. This current is often several amps even for small, low powered motors. The semiconductor driver must be able to pass this current without being damaged. As the motor starts to rotate, the armature coils which are moving in a magnetic field, generate their own voltage. This opposes the applied voltage and reduces the overall current flowing. So the current passing through the motor when it is rotating is much less than the initial start up current.

The direction of rotation of a dc motor is dependent upon the direction of the current passing through the motor. A convenient way of being able to change the direction of rotation of a motor is to use a relay with two sets of change-over contacts (double pole, double throw). The circuit diagram of such a circuit is shown in figure 7.4
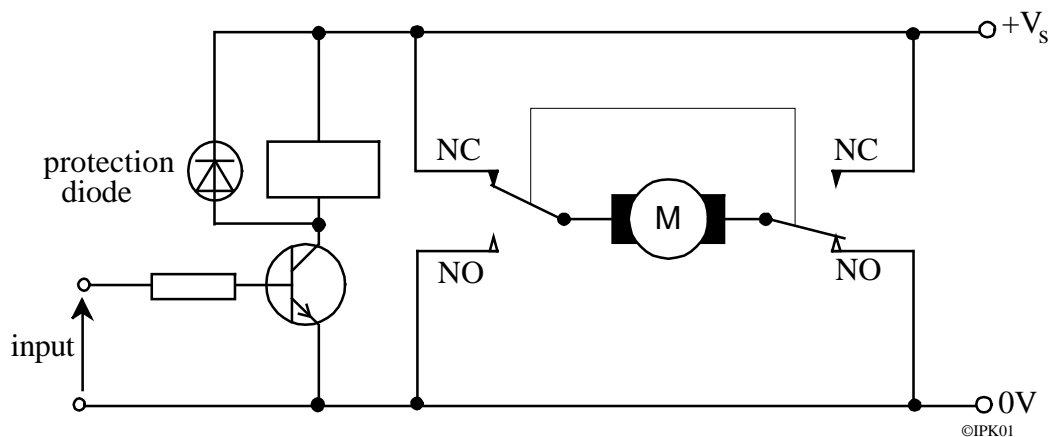
Figure 7.4

It is a useful exercise to verify that the direction of rotation of the motor will change when an input is applied to the circuit.

10.8 OPERATIONAL AMPLIFIERS

Although a logic gate is able to decide whether an analogue voltage is below or above a specific value (a logic 0 or a logic 1), there is a region of uncertainty about this fixed specific value which is often as much as several hundred millivolts. The operational amplifier, when used as a comparator, overcomes these problems.

An operational amplifier (op-amp) is a voltage amplifier which amplifies the difference between the voltages on its two input terminals. Op-amps are often require a dual balanced d.c. power supply, eg ± 15V. The power supply connections are often omitted from circuit diagrams for simplicity. Figure 8.1 shows the typical connections for an op-amp.
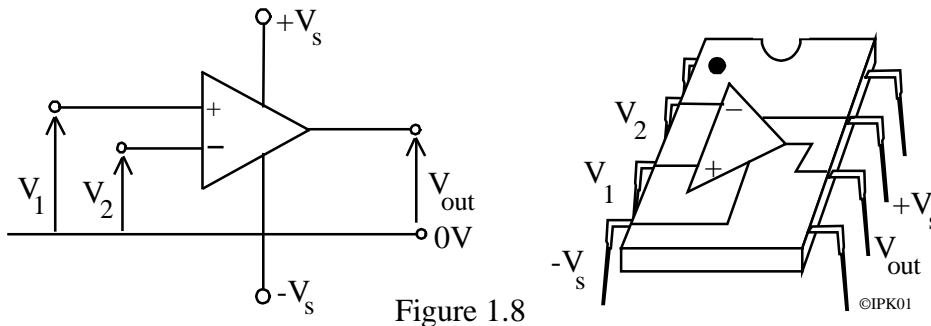
Figure 1.8

The + input terminal is known as the non-inverting input and the – input terminal is known as the inverting input terminal.
The output voltage is given by

$$V_{out} = A(V_1 - V_2)$$

A is the open loop voltage gain, i.e. when there is no feedback.

For the purposes of the written tests, the op-amp is assumed to behave ideally i.e.
- the open loop gain is very large (in practice it is only very large at low frequencies),
- the maximum output voltage is equal to the power supply voltage, (in practice it is about 2V less),
- it has infinite input impedance so no current passes into the input terminals, (in practice the input impedance is not infinite so there is a current of a few nano-amps),
- the output impedance is zero so it can supply any required current, (in practice the op-amp is designed to limit the current to a few milliamps),
- the output voltage is zero when the two inputs are equal, (in practice there is a small offset voltage which needs a variable resistor to balance out).

In practice an op-amp is frequency compensated for stability internally by a low value capacitor connected between the inverting input terminal and the output terminal. The voltage gain decreases as the frequency increases as shown in figure 8.2.
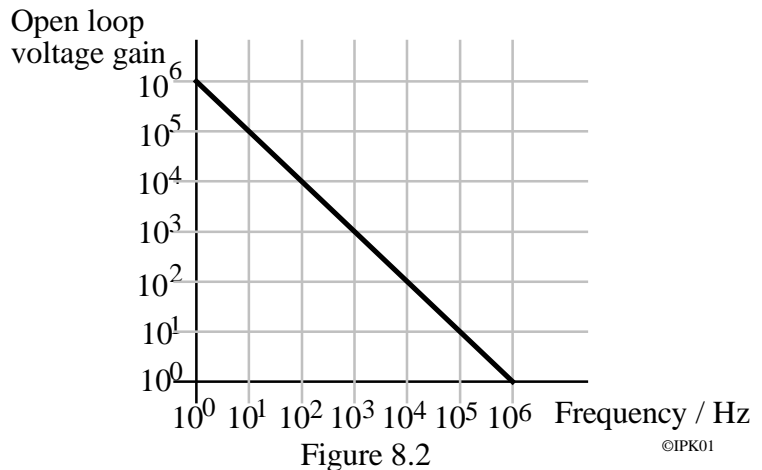
Figure 8.2

The Op-Amp As A Voltage Comparator

The output voltage of an op-amp is given by

$$V_{out} = A(V_1 - V_2)$$
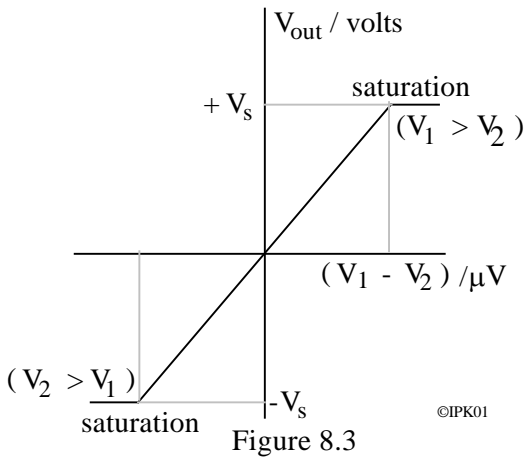
Figure 8.3

Since the op-amp has a very large open loop gain, A, only a very small difference between V_1 and V_2 is needed for the output to be saturated. The transfer characteristic for an op-amp is shown in figure 8.3. This characteristic enables the op-amp to compare the two voltages on its input terminals.

If V_1 is greater than V_2 the output saturates at the positive supply voltage. If V_2 is greater than V_1 the output saturates at the negative supply voltage. This principle can be used to compare two voltages, a reference voltage and a varying input voltage.

$$V_1 \rangle V_2 \Rightarrow V_{out} = +V_s$$

$$V_2 \rangle V_1 \Rightarrow V_{out} = -V_s$$

An op-amp can be used as a comparator either with a dual power supply or with a single power supply. Both are considered below, as each have their own specific problems when used with real op-amps.

Dual Power Supply Comparator

Consider the circuit diagram in figure 8.4.

Figure 8.4
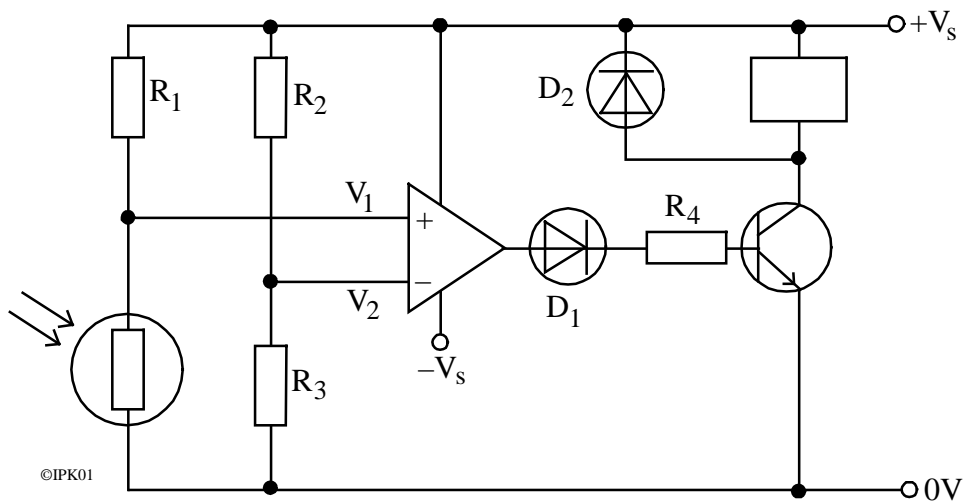
The op-amp operates from $+V_s$ and $-V_s$ but the rest of the circuit operates from just $+V_s$. Resistors R_2 and R_3 set the voltage at the op-amp inverting input terminal which then sets the reference voltage for the non-inverting input terminal. If R_2 is equal to R_3, then the reference voltage will be $+\frac{1}{2}V_s$.

Resistor R_1 forms a voltage divider with the LDR; the voltage to the non-inverting input of the op-amp being larger than the reference voltage when the LDR is in the dark.

When the LDR is in the dark, V_1 is greater than V_2 and so the output of the op-amp saturates at the positive supply voltage, $+V_s$. (In practice the output of the op-amp will be approximately 2 volts less than the supply voltage). Diode, D_1 conducts and the resistor R_4 limits the current passing into the base of the transistor. The transistor will be switched on, which in turn will switch on the relay. The relay could be used to power a large lamp, ie so that when it is dark the circuit switches on a lamp. Diode D_2 is there to protect the transistor from the large induced voltage produced when the relay is switched off.

When the LDR is in the light, V_2 is greater than V_1 and so the output of the op-amp saturates at $-V_s$ (in practice $-V_s + 2$ volts). If this negative voltage were applied to the base of the transistor, it could cause damage to the base-emitter junction of the transistor (it can make it behave like a zener diode). Diode D_1 prevents this happening becasue it is reverse biased for negative voltages. The transistor and relay are therefore switched off.

The actual light intensity at which the relay switches is determined by considering the voltages V_1 and V_2. As an example, if $R_1 = R_2 = R_3 = 10k\Omega$ and the LDR has the same characteristic as in figure 5.1, then the relay will switch when $V_1 = V_2$, ie when the LDR has a resistance of $10k\Omega$. This occurs when the light intensity is 100 lux.

Single Power Supply Comparator

Consider the circuit diagram in figure 8.5.
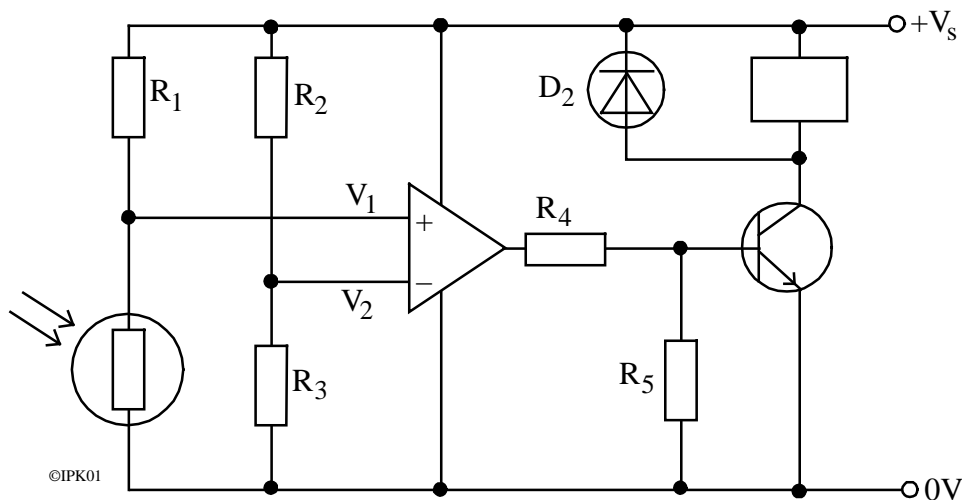
Figure 8.5

It is essentially the same as the circuit for the dual supply except that diode D_1 is no longer needed. If the op-amp behaved in an ideal manner its output would be at 0V when $V_2 > V_1$. In reality, the output of the op-amp will never be less than approximately 2 volts. If R_5 were not present, the transistor would therefore be permanently switched on. R_5 has to be chosen so that when the output of the op-amp is at its lowest voltage, the voltage at the base of the transistor must be less than approximately 0.6V.

There are other possible solutions to the problem of op-amps not saturating at 0V, including the use of a zener diode or a LED in series with resistor R4. The circuit using an LED is shown in figure 8.6. When the circuit is in use, the LED will always be illuminated, though its brightness will change depending upon whether the output of the op-amp is high or low.
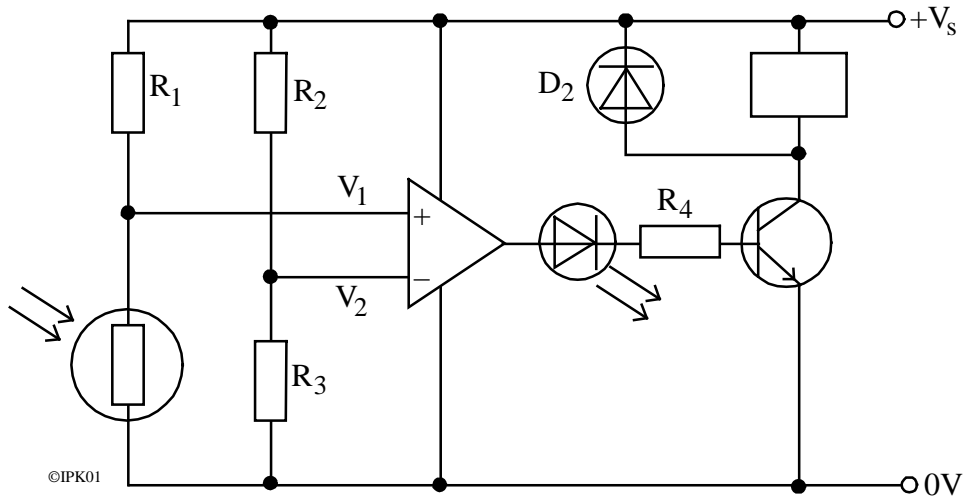
Figure 8.6

10.9 CAPACITORS

With all of the systems considered so far, the output changes as soon as there is an appropriate change in input. For some applications this is unsuitable and it would be more appropriate for the output to change some time after the input change has occurred. In other applications it could be appropriate for the output to revert back to its initial state after a certain time has elapsed, even if the input has not changed. In order to implement these timing functions it is necessary to use capacitors.

Figure 9.1 shows the construction of capacitors.

Figure 9.1
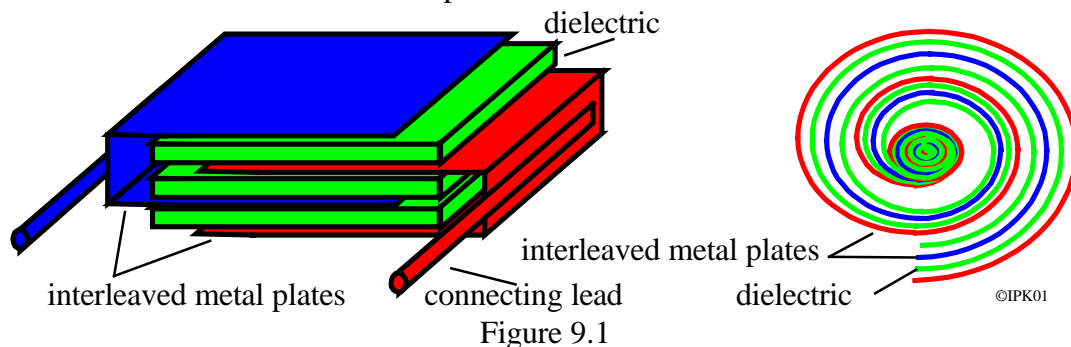
A capacitor consists of two overlapping conducting plates separated by an insulator called the dielectric. The separation of the two plates is often very small. When a voltage, V, is applied across the two conducting plates they store electrical charge, Q (+Q on one plate and –Q on the other). The charge stored per volt is called the capacitance, C.

$$\Rightarrow \ C \ = \ \frac{Q}{V}$$

The unit of capacitance is the farad (F). This is the capacitance required to store a charge of 1 coulomb when there is a voltage of 1 volt across the plates.
This is a very large unit and sub-units are used:-

$$1 \text{ microfarad } \ (1\,\mu F) \ = 1 \times 10^{-6} F$$
$$1 \text{ nanofarad } \ (1\,nF) \ = 1 \times 10^{-9} F$$
$$1 \text{ picofarad } \ (1\,pF) \ = 1 \times 10^{-12} F$$

The capacitance increases when:
> the area of overlap of the plates is increased,
> the distance between the plates is decreased,
> an insulator (dielectric) with a higher dielectric constant is used.

When selecting capacitors for a particular use, the factors to be considered are as follows:
> the capacitance
> the tolerance
> the working voltage   (This is the largest voltage which can be applied across the plate before the dielectric breaks down and conducts.)
> the leakage current   (No dielectric is a perfect insulator but the loss of charge through it should be small.)

The Markings On A Fixed Capacitor
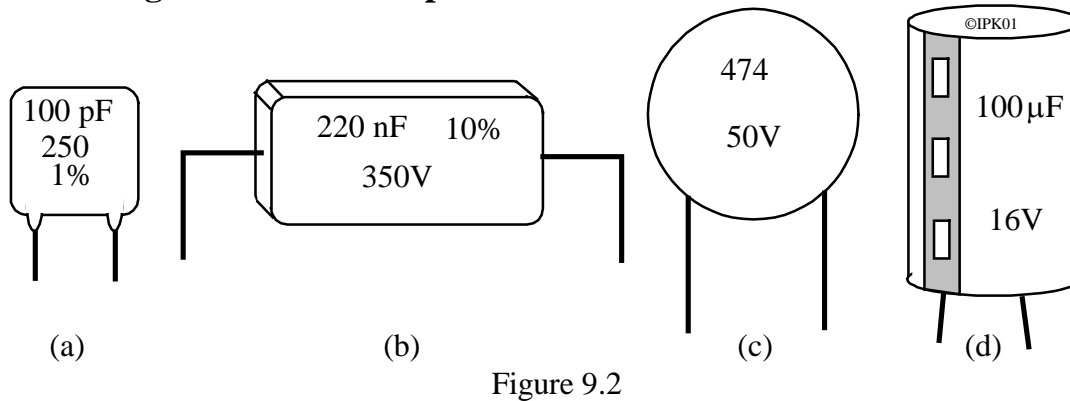
Figure 9.2

Figure 9.2 shows some typical component outlines of capacitors and the typical markings found on them.

Types (a) and (b) are typical of close tolerance capacitors which have their value, working voltage and tolerance marked.

Type (c) represents a ceramic capacitor with its value ($474 \equiv 470000pF \equiv 0.47\mu F$) and working voltage marked.

Type (d) represents an electrolytic capacitor and has its value, maximum working voltage and polarity marked.

Electrolytic capacitors are made by electrolysis; the two plates are coated with liquid and a current passed between them. This forms a very thin layer of dielectric on one plate. Electrolytic and tantulum capacitors are polarised and must be connected the correct way round.

As a result of the small size of surface mounted resistors and capacitors, their values are identified by a number, as shown in figure 9.3.
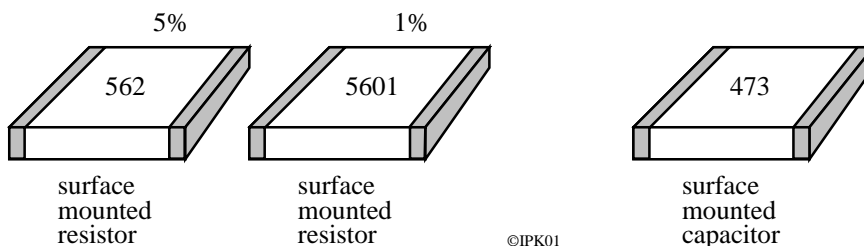
Figure 9.3

The code used for the value consists of three numbers for a 5% (or greater) tolerance or four numbers for a 1% tolerance. The first two (or three) numbers give the significant figures of the value and the third (or fourth) figure gives the multiplier.

eg. in the surface mounted resistors in figure 9.3 the value of the 5% device is $5\,600$ ohms
i.e. $5.6k\Omega$

The 1% resistor has the same value $5\,600$ ohms i.e. $5.60k\Omega$

For capacitors the value is given in picofarads (pF), so the value is $47\,000pF$
i.e. 47nF or $0.047\mu F$

For an ideal capacitor direct current does not pass through it since there is an insulator separating the metal plates that form the capacitor. However, if a voltage larger than the insulator will withstand (the working voltage) is applied, then the electrons will have enough energy to break through the insulator and cause a current to pass. Any passage of current will cause energy to be dissipated and so the capacitor will be rapidly destroyed. It is very important therefore, to ensure that the maximum working voltage of a capacitor is greater than the voltage that the capacitor will actually experience.

Large valued capacitors using separate metal plates and insulators will be physically large. In order to produce large valued capacitors with a small physical size it is necessary to use a different technique. This consists of using thin aluminium foil for the plates. This foil has a chemical coating which causes a layer of aluminium oxide to form between the plates which acts as the dielectric. This oxide layer is produced by electrolysis, which means that there must be a small current passing between the plates. In other words, the capacitor must have a leakage current to maintain the dielectric and the capacitor is therefore polarised, i.e. it must be connected the correct way round in the circuit. Such capacitors are known as **electrolytic** capacitors. Usually the negative terminal is marked with

Electrolytic capacitors have the following weaknesses:
- poor tolerance (often $\pm 50\%$) of their stated value,
- poor stability (the value changes with time),
- poor high frequency response as a result of the tightly coiled aluminium plates,
- noise which is introduced by the leakage current and
- a leakage current can interfere with critical timing circuits.

They are, however, the only way to obtain large value capacitors that are physically small. Capacitors made from Tantalum have better characteristics than normal electrolytic capacitors but are considerably more expensive.

Electrolytic capacitors are mainly used for smoothing and decoupling (removal of high and low frequency signals) from power supplies. Wherever possible, their use in the signal path of circuits should be avoided so as to minimise signal distortion. Non polarised capacitors should be used instead.

Uses Of Capacitors

- smoothing out variations in power supplies,
- removing alternating signals,
- blocking the passage of direct current while allowing the passage of alternating current,
- combination with inductors for resonant tuned circuits,
- combination with resistors as charging and discharging circuits.

Two Capacitors In Series

When two capacitors are connected in series in a circuit the same charge is stored in both. The applied voltage, V, is the sum of the voltages across the separate capacitors:

$$\mathbf{V = V_1 + V_2}$$

Using the equation $\mathbf{C = \dfrac{Q}{V}}$ the resulting capacitance is found from

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$
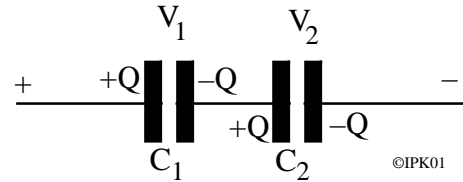
Figure 9.4

Two Capacitors In Parallel

When two capacitors are connected in parallel, the voltage, V, across each capacitor is the same.
The total charge stored, Q, is equal to the sum of the charges stored in the separate capacitors.

$$\mathbf{Q = Q_1 + Q_2}$$

Figure 9.5

Using the equation, $\mathbf{C = \dfrac{Q}{V}}$, the resulting capacitance is found from:

$$\mathbf{C = C_1 + C_2}$$
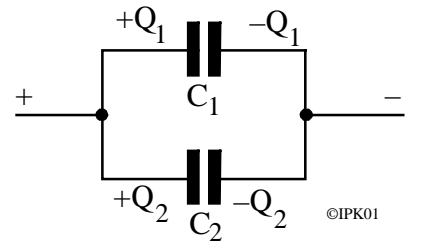
10.10   RC NETWORKS (dc only)

For capacitors to actually be used in timing circuits it is necessary to consider how the voltage across a capacitor varies with time when the current in the circuit is being limited by a resistor.

Consider the circuit shown in figure 10.1.
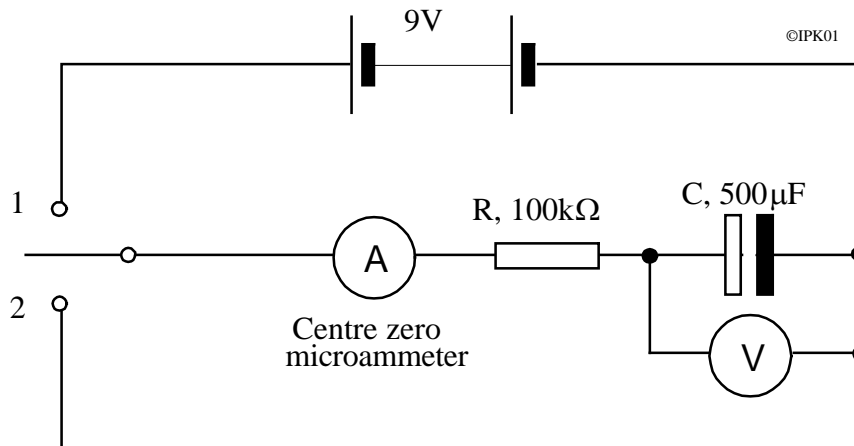
Figure 10.1

With the switch in position 1 the graphs in figure 10.2, are obtained for the current in the circuit and the voltage across the capacitor, as the capacitor charges.
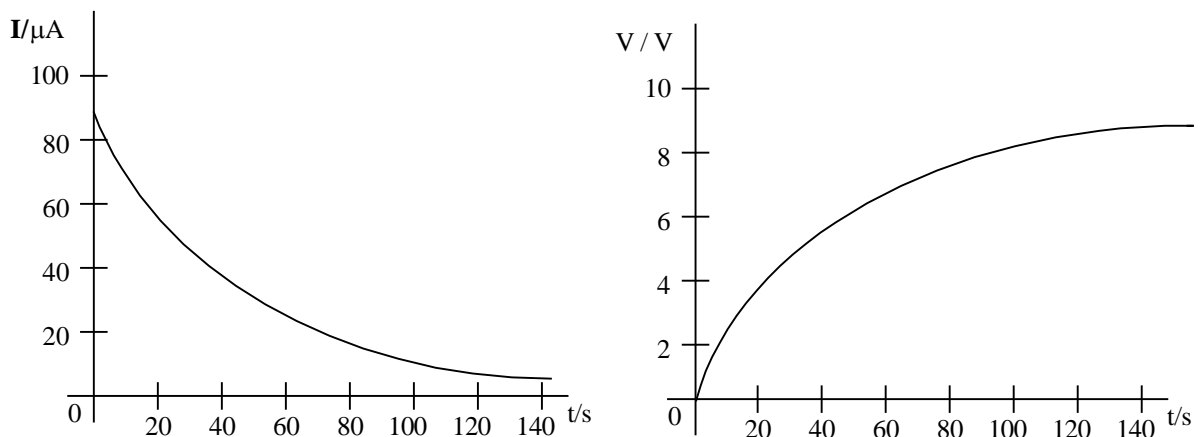
Figure 10.2.

With the switch in position 2 the corresponding graphs are obtained for the discharge as shown in figure 10.3.
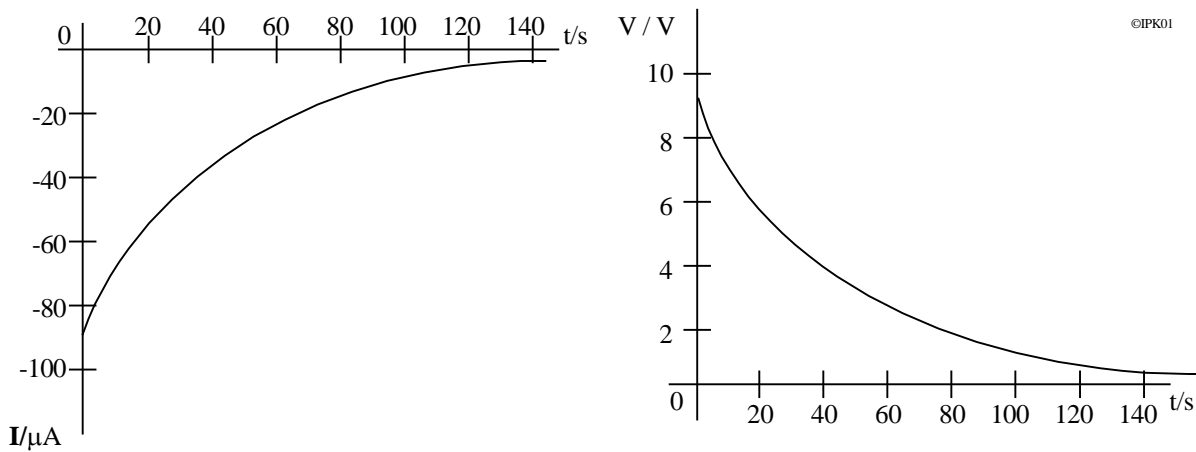
Figure 10.3

Analysis of the graphs shows:

On charging or discharging, the current I in the circuit is maximum at the start and decreases more and more slowly until it finally becomes zero. On discharging, the current is in the opposite direction to when charging.

On charging, the voltage, V, across the capacitor rises rapidly from zero and slowly approaches its maximum value when the capacitor is fully charged and I is zero.

On discharging, the voltage, V, falls rapidly from its maximum value and slowly approaches zero when the capacitor is fully discharged.

The **time constant** for the circuit, T, defined as RC, is the time taken to discharge to **37%** of the initial voltage or to charge to **63%** of the final voltage. The derivation of these values is not required.

$$T = RC$$

The time **5RC** is taken as the time to charge or discharge completely.

The time taken to charge or discharge to half of the supply voltage is **0.69RC**

Timing Circuits

A simple timing circuit is shown in figure 10.4. When the push switch is pressed, the capacitor charges very quickly so that the voltage across it is $+V_s$ and the LED lights. When the switch is released the capacitor discharges through R_2 and keeps the transistor switched on. When the voltage across the base-emitter junction of the transistor becomes less than 0.7V, the LED is switched off. The time taken for this to occur depends upon the supply voltage, the capacitor and the resistor R_2.

Figure 10.4

If V_s is 9V, C is 100μF and R_2 is 100kΩ, then the time taken for the LED to switch off is about 6 seconds.

A serious disadvantage of this circuit is that there is no definite switch off point for the LED, instead it just becomes dimmer and dimmer.
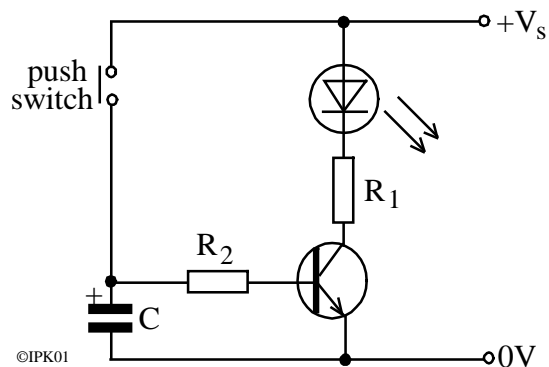
A better timing circuit uses a logic gate as the switching device since it has more definite switching characteristics. Such a circuit is shown in figure 10.5.
In this circuit the LED will light when the switch is pressed and remain on until the voltage across the capacitor decreases to less than half of the supply voltage. The time taken for this will be approximately 0.7RC.
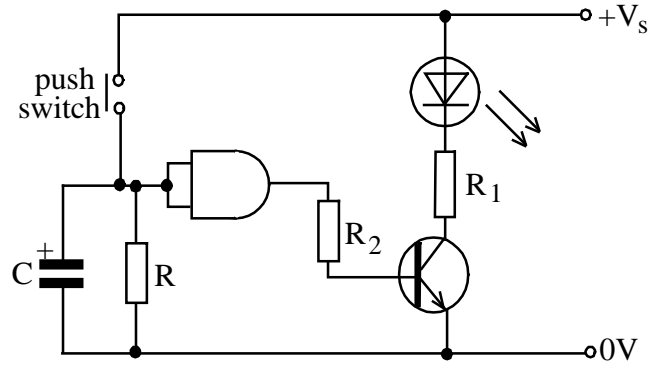
Figure 10.5 ©IPK01

The circuit in figure 10.6 shows how a change in an input can be delayed from acting on the output. The circuit is a variant of figure 8.5.
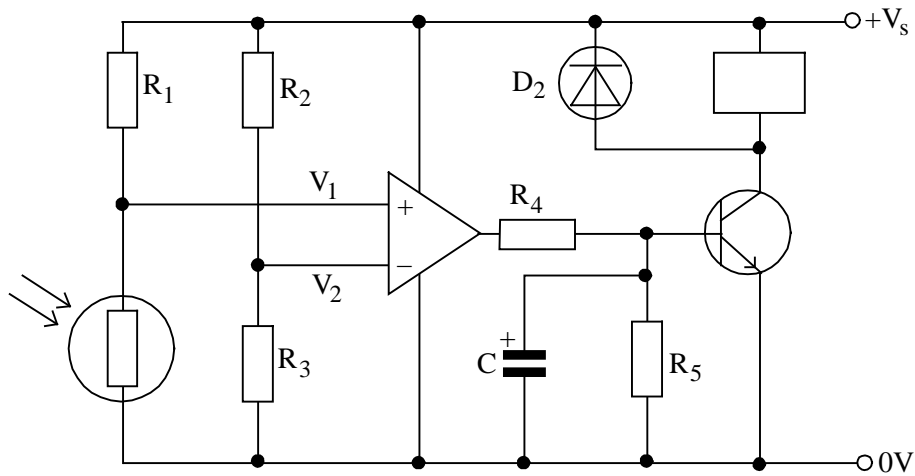
Figure 10.6 ©IPK01

The time delay for the relay to switch on is determined by the value of R_4, C and V_s. The time delay in the relay switching off will depend on R_4, R_5, C and V_s.

Figure 10.7 shows how the circuit above could be modified so that when the output of the op-amp goes high, the relay switches on, but only for a set time.
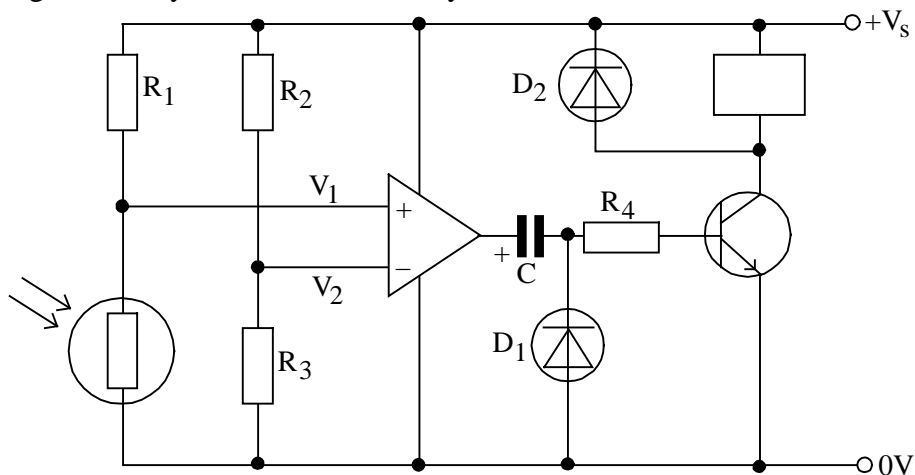
Figure 10.7 ©IPK01

When the output of the op-amp goes high, the capacitor will charge through R_4 and the base-emitter junction of the transistor and the transistor will be switched on. When the capacitor is charged, the transistor will switch off. Diode D_1 helps the capacitor to discharge when the op-amp output goes low.

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10.11   THE 555 TIMER IC

The timing circuits shown in the previous section are all relatively inaccurate and it is difficult to predict the actual time periods that will occur. A much better solution is to use a dedicated timing IC, the 555.

This very versatile integrated circuit was first produced in 1973. The circuit and its derivatives are still used in large quantities. While it is not necessary to know the internal structure of this device, it does aid understanding if the main internal features are known. These are as follows:

- three precision resistors connected in series across the power supply as a voltage divider and so giving voltages of $\frac{1}{3}V_S$ and $\frac{2}{3}V_S$, where V_S is the supply voltage;

- two comparators, one switching at $\frac{1}{3}V_S$ via the TRIGGER input and the other switching at $\frac{2}{3}V_S$ via the THRESHOLD input;

- a latch, SET by the output of the TRIGGER comparator and RESET by the output of the THRESHOLD comparator;

- a high current output capable of sinking or sourcing 200mA;

- an open collector transistor switch, which connects the DISCHARGE terminal to 0V when the output terminal is at 0V.

The pin diagram for a 555 timer IC is shown in figure 11.1.

©IPK01
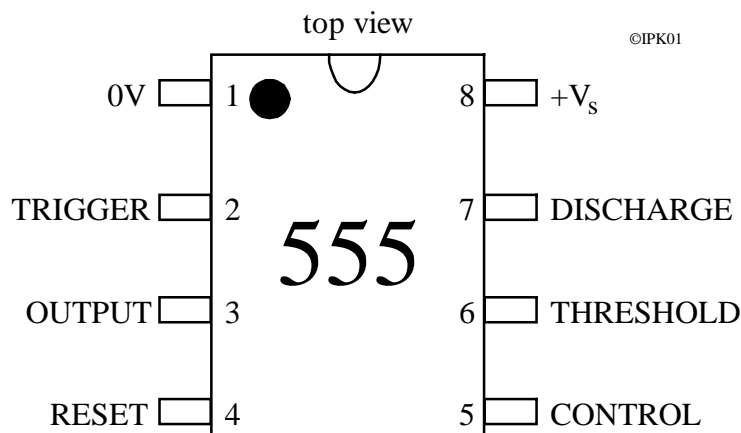
Figure 11.1

The operation of a 555 can be summarised as follows.

If the voltage at the TRIGGER input is less than $\frac{1}{3}V_S$ then the output goes to V_S and remains there until the voltage at the THRESHOLD input rises above $\frac{2}{3}V_S$, at which value the output is set to 0V.

The RESET terminal can be used to set the output to 0V at any time by being connected momentarily to 0V. Normally, the RESET terminal is connected to V_S to prevent any spurious resetting of the output.

The CONTROL terminal is connected to the $\frac{2}{3}V_S$ point of the voltage divider and can be used to alter the voltage switching levels of the comparators. Normally it is decoupled by a 10nF capacitor connected to 0V.

The 555 Monostable

A monostable is a circuit which, having received a trigger signal, produces an output for a predetermined time. It has one stable state and one unstable state.
The circuit diagram for a 555 monostable is shown in figure 11.2.
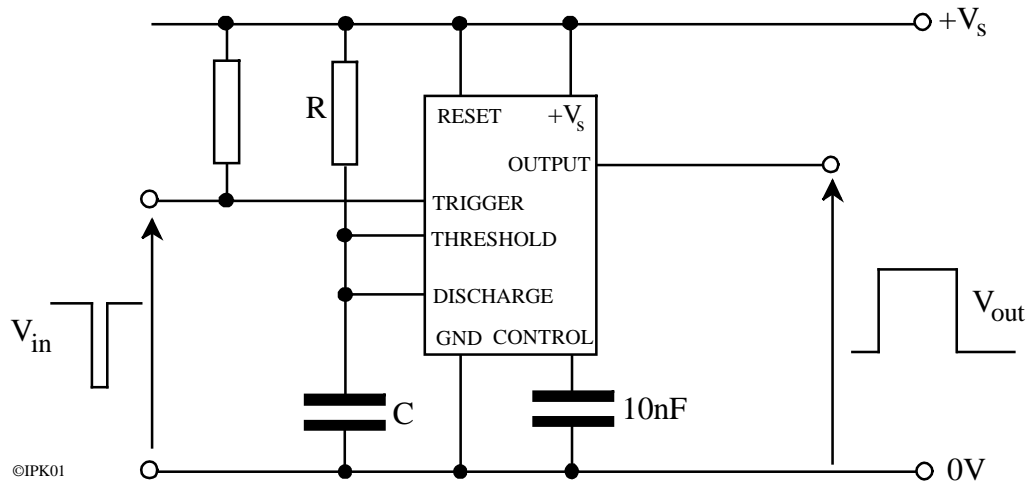
Figure 11.2

The resistor connected to the TRIGGER input ensures that it is held above $\frac{1}{3}V_S$ in the absence of an input signal. Typically the value of this resistor would be 10kΩ or greater; its value is not critical. Before being triggered, the output of the monostable is at 0V, and the DISCHARGE terminal of the 555 is also at 0V, ensuring that the timing capacitor is discharged.

When V_{in} goes below $\frac{1}{3}V_S$, the output voltage, V_{out}, becomes V_S and the DISCHARGE terminal becomes open circuit, so allowing the capacitor, C, to charge through resistor R. The output will stay at V_S until the voltage across C becomes greater than the threshold switching voltage, $\frac{2}{3}V_S$. When this happens, the output voltage will return to 0V and the DISCHARGE terminal will again connect to 0V, so discharging C very quickly. This state is STABLE and the circuit will remain like this until V_{in} becomes less than $\frac{1}{3}V_S$.

In theory any combination of R and C is possible to achieve a required time period. In practice, however, there are several things to remember.

> The transistor connected to the DISCHARGE terminal, as well as having to conduct the short-circuit current of the timing capacitor when the monostable resets, also has to carry the current flowing through the timing resistor. To prevent destruction of this transistor the minimum value of R should be 1kΩ.

> The minimum value of C should be considered as 100pF, since any smaller value will be similar to the input capacitance of the timer circuit and so the time periods will be inaccurate.

> There are two factors to consider when looking at the maximum value of C. The first is that any large value capacitors will be electrolytic and so have a leakage current which must pass through R. If the leakage current is too large for the value of R then the time period will be inaccurate. It could well happen, if there is a large leakage current, that the voltage across C never reaches $\frac{2}{3}V_S$ and so the threshold switching voltage level is *never* reached!

The second factor is the current that will pass through the discharge transistor at the end of the timing period. If the short circuit current is too large then the transistor will be destroyed. The maximum value of C should therefore be limited to 1000μF.

All electrolytic capacitors are inaccurate and their values change with time, so accurate time periods cannot be produced by monostable circuits with electrolytic capacitors. Tantalum bead capacitors will give a little more accuracy and stability than normal electrolytics.

The THRESHOLD input requires a current of a few μA, so this, combined with the leakage current of the capacitor C, needs to be taken into account when using very large values for R. In practice it is worth limiting the maximum value of R to 1MΩ.

Taking all these factors into account, the minimum time period of a 555 monostable is about 0.1μs and the maximum time period is approximately 1000s.

For the **monostable,** the time that the output voltage is at V_s is calculated by using the formula.

$$T = 1.1 \times R \times C$$

where T is in seconds, R is in ohms and C is in farads.

For example, if R has a value of 100kΩ and C has a value of 100μF then the time for which the output will be at the supply voltage is

$$T = 1.1 \times 100000 \times 0.0001 = 11 \, seconds.$$

The 555 Astable

An astable circuit has no stable states but continuously switches from a high output to a low output. The common circuit for a 555 astable is shown in figure 11.3.
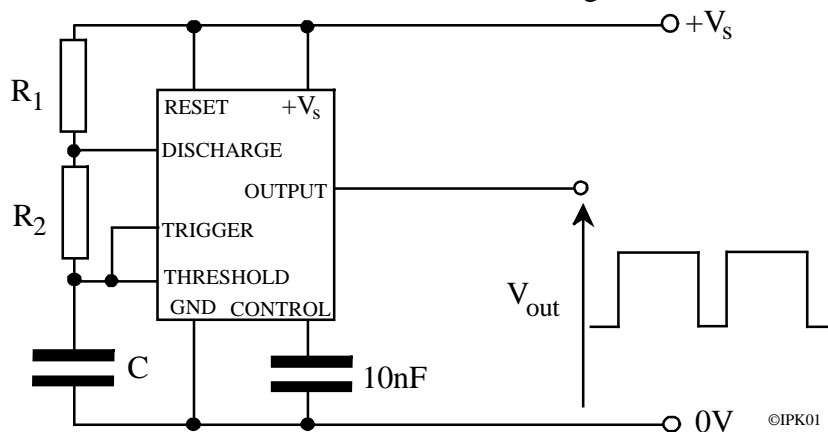
Figure 11.3

When first switched on the capacitor, C, is discharged and so the voltage across this capacitor is less than the TRIGGER voltage and so the output goes to V_s. The capacitor, C, charges through R_1 and R_2 until the voltage across C is greater than the THRESHOLD switching level, at which point the output voltage becomes 0V and the DISCHARGE terminal becomes connected to 0V.

The capacitor now discharges through R_2 until the voltage across C becomes less than the TRIGGER switching voltage. When this happens, the output voltage becomes V_s and the process repeats. It should be noted that the first pulse is longer than the remainder, since C has to charge from 0V and not $\frac{1}{3}V_s$. The same restrictions apply to the values of C and R (R_1 and R_2) as for the monostable.

The timing diagram for the astable is shown in figure 11.4.
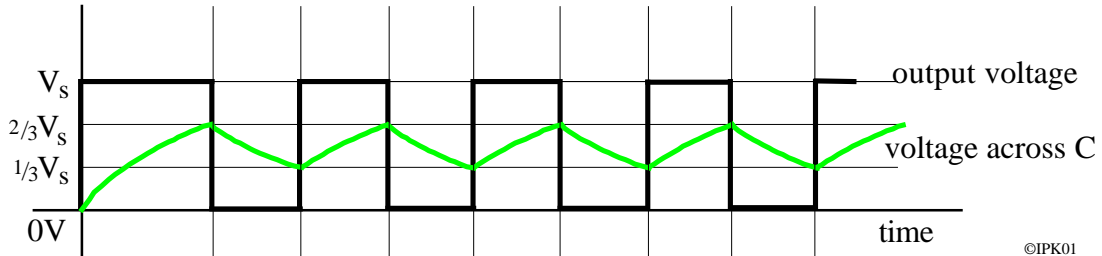
Figure 11.4

The time that the output is high can be calculated from

$$t_H = 0.7(R_1 + R_2)C$$

and the time that the output is low can be calculated from

$$t_L = 0.7 R_2 C$$

The timing period is given by

$$T = 0.7(R_1 + 2R_2)C = \frac{(R_1 + 2R_2)C}{1.44}$$

For example, if R_1 has a value of 100kΩ, R_2 has a value of 47kΩ and C has a value of 100nF then the time period is

$$T = \frac{(100000 + 2 \times 47000) \times 0.0000001}{1.44}$$

$$\Rightarrow T = \frac{194000 \times 0.0000001}{1.44} = 0.0135s.$$

But

$$frequency = \frac{1}{time \ period}$$

So the frequency of the astable circuit is given by

$$f = \frac{1.44}{(R_1 + 2R_2)C}$$

and so for the above example the frequency will be **74.1Hz.**

With the usual circuit for a 555 astable it is not possible to obtain a square waveform, i.e. when the output is at the supply voltage for as long as it is at 0V.

It might be thought that this could be achieved by making R_1 equal to zero (to make **t_H** and **t_L** equal). If this is attempted, then as soon as the output goes low the DISCHARGE terminal is connected to 0V, so short circuiting the power supply and damaging the DISCHARGE transistor.

The minimum value for R_1 should be considered to be 1kΩ. If, however, R_2 has a value of 1MΩ then the error in the ratio of the time for which the output is high to that for which the output is low (mark to space ratio) will be about 0.1%, which may well be adequate.

The only way to obtain a mark to space ratio of exactly 1:1 is by the use of frequency division which is considered in the next module.

As a result of the internal construction of the 555 IC, the output voltage does not, in practice, actually equal $+V_S$. The actual voltage will depend upon the current flowing through the output, but even with only a current of a few mA, the actual high output voltage is approximately 1V less than $+V_S$.

11.1 DESIGN AND SIMPLIFICATION OF COMBINATIONAL LOGIC SYSTEMS

A logic system is usually designed to satisfy a description or specification for an intended process or operation.

Consider the logic system needed to decode a four bit binary number so that its value could be indicated on a 7 segment array. Such an array is shown alondside with the segments labelled **a** to **g**.

To design this system, each segment is considered separately and the conditions under which each segment is lit clearly defined.

The electronics engineer will have to translate these conditions into a working circuit that is reliable but also as cheap to produce as possible.

One possible way of implementing this would be to use a dedicated IC or a microprocessor control system using a PIC or AVR controller. This approach will be considered in Module 3. For now, a solution based on logic gates will be used.
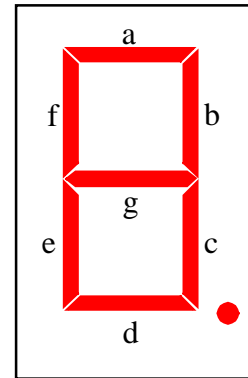
Figure 4.3

Consider segment **e**. It has to be lit when the numbers 0, 2, 6 and 8 are displayed. If A, B, C, and D represent the binary inputs, with A representing the least significant and D the most significant bit, then the truth table for **e** is

D	C	B	A	e
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

It would be very difficult to produce a subsystem for lighting **e** directly from the truth table so it is usual to translate the truth table into a Boolean equation or expression. To do this each row where **e** is a "**1**" is written as an **AND** expression. The top row of the table represents the input for 0 and so D = 0, C = 0, B = 0 and A = 0. For these to form a logic 1 when **AND**ed together requires the inverse of each of these terms to be used

$$\text{i.e.}\ \ \overline{D}\cdot\overline{C}\cdot\overline{B}\cdot\overline{A}\,.$$

This is repeated for the other three conditions that **e** is to be lit and then they can be **OR**ed together to form the complete expression for **e**.

$$e = \overline{D} \cdot \overline{C} \cdot \overline{B} \cdot \overline{A} + \overline{D} \cdot \overline{C} \cdot B \cdot \overline{A} + \overline{D} \cdot C \cdot B \cdot \overline{A} + D \cdot \overline{C} \cdot \overline{B} \cdot \overline{A}$$

Before constructing the logic subsystem from the Boolean equation it is always good practice to see whether the equation can be simplified. Using the Distributive Law (see page 15 of the Foundation Module support booklet) the first and last terms of the equation can be combined as

$$e = (\overline{D} + D) \cdot \overline{C} \cdot \overline{B} \cdot \overline{A} + \overline{D} \cdot \overline{C} \cdot B \cdot \overline{A} + \overline{D} \cdot C \cdot B \cdot \overline{A}$$

but $\overline{D} + D = 1$

$$\Rightarrow e = \overline{C} \cdot \overline{B} \cdot \overline{A} + \overline{D} \cdot \overline{C} \cdot B \cdot \overline{A} + \overline{D} \cdot C \cdot B \cdot \overline{A}$$

which has successfully removed one complete term and simplified another. The same process can also be applied to the two remaining 4-bit terms giving

$$\Rightarrow e = \overline{C} \cdot \overline{B} \cdot \overline{A} + (\overline{C} + C) \cdot \overline{D} \cdot B \cdot \overline{A}$$

but $\overline{C} + C = 1$

$$\Rightarrow e = \overline{C} \cdot \overline{B} \cdot \overline{A} + \overline{D} \cdot B \cdot \overline{A}$$

This is obviously more appropriate for construction than the first expression produced for **e**. It can be further simplified by taking $\overline{A}$ out of both terms giving

$$\Rightarrow e = (\overline{C} \cdot \overline{B} + \overline{D} \cdot B) \cdot \overline{A}$$

which could now be constructed from two input logic gates.

More Boolean Identities

Consider the truth table, shown below, for a two input **NOR** gate.

B	A	$Q = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

If the complement of the two inputs were used instead, then the truth table becomes

$\overline{B}$	$\overline{A}$	Q
0	0	0
0	1	0
1	0	0
1	1	1

This has the same form as the truth table for an AND gate i.e.

$$\overline{\overline{A} + \overline{B}} = A \cdot B$$

$$\overline{A} + \overline{B} = \overline{A \cdot B}$$

This is one of the theorems discovered by Augustus De Morgan who was a friend of George Boole. His second theorem can be demonstrated in a similar way and is

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

Both of these can be extended to include as many variables as required i.e.

$$\overline{A + B + C + D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$$

and

$$\overline{A} + \overline{B} + \overline{C} + \overline{D} = \overline{A \cdot B \cdot C \cdot D}$$

De Morgan's theorems are useful for simplifying Boolean expressions for logic systems and can be used to convert **OR** functions to **AND** functions or vice versa. This can be particularly useful when, for example, an **OR** function is required but there are unused **NAND** gates on the circuit board.

It is a useful exercise to use De Morgan's theorems to work out how a **NAND** gate can be made from three **NOR** gates and also how a **NOR** gate can be made from three **NAND** gates.

Karnaugh Maps.

Karnaugh maps represent an alternative method for depicting and simplifying logic systems. They can be considered as a truth table that has been turned inside out and as such, displays the output of the logic system in a more visual and accessible manner. As usual **A**, **B**, **C**, **D**, etc. represent inputs and **Q** represents the output.

Consider the truth table shown below, for a two input **AND** gate.

B	A	Q
0	0	0
0	1	0
1	0	0
1	1	1

If the table is turned inside out with **A** and **B** forming the horizontal and vertical column headings respectively, then the output states, **Q**, can be written inside the table. This representation is called a Karnaugh map and is shown below for the truth table above.

```
      A
  B \  0   1
  0 | 0 | 0 |
  1 | 0 | 1 |
```

Karnaugh maps for all of the other two input logic gates can be produced in a similar way by having the row and column headings as the input states and then filling in the table with the output states, Q.
e.g.

```
    A                A                A                A
 B \ 0  1         B \ 0  1         B \ 0  1         B \ 0  1
 0 | 0 | 1 |      0 | 1 | 1 |      0 | 1 | 0 |      0 | 0 | 1 |
 1 | 1 | 1 |      1 | 1 | 0 |      1 | 0 | 0 |      1 | 1 | 0 |
     OR               NAND             NOR              EXOR
```

A similar system can be used to represent three, four (and even greater) input logic gates. For these, two (or more) inputs are combined to form the rows and columns.
The truth table for a three input **AND** gate is shown below.

C	B	A	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

The Karnaugh map for this **AND** gate is shown below.

```
        BA
  C╲  00  01  11  10
  0 │ 0 │ 0 │ 0 │ 0 │
  1 │ 0 │ 0 │ 1 │ 0 │
```

NOTE: For the simplification process used later in this section to work, the dual labels for **BA** must only change by one binary digit at a time. The labels for **BA** are therefore *NOT* in binary order.

Similarly a four input **AND** gate has the following truth table and Karnaugh map.

D	C	B	A	Q
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

```
          BA
   DC╲  00  01  11  10
   00 │ 0 │ 0 │ 0 │ 0 │
   01 │ 0 │ 0 │ 0 │ 0 │
   11 │ 0 │ 0 │ 1 │ 0 │
   10 │ 0 │ 0 │ 0 │ 0 │
```

NOTE: The row labels now have the same form as those of the columns with only one binary digit changing at a time. This is important if the simplification process is to work.

Consider again the logic system needed to decode a four bit binary number so that its value could be indicated on a seven segment array. Such an array is shown opposite with the segments labelled **a** to **g**. Segment **e** is lit for the following numbers:-
0, 2, 6, 8
The truth table for this is redrawn below.
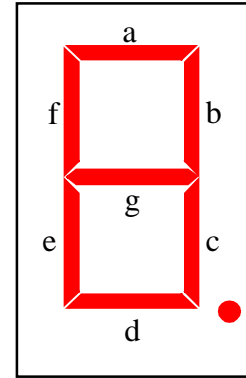
D	C	B	A	e
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

The Boolean expression for this is

$$e = \overline{D}\cdot\overline{C}\cdot\overline{B}\cdot\overline{A} + \overline{D}\cdot\overline{C}\cdot B\cdot\overline{A} + \overline{D}\cdot C\cdot B\cdot\overline{A} + D\cdot\overline{C}\cdot\overline{B}\cdot\overline{A}$$

The Karnaugh map for this is

To begin the simplification process it is necessary to look in the Karnaugh map for horizontally or vertically adjacent "**1**s".
In this map there is only one apparent such occurrence and that is ringed in the map drawn below

This shows that when **D = 0**, **B = 1** and **A = 0**, **e** is **on** (**1**) irrespective of whether **C = 0** or **1**.
This term therefore becomes $\overline{\mathbf{D}} \cdot \mathbf{B} \cdot \overline{\mathbf{A}}$
Taking the remaining terms from the Karnaugh map where there is a **1** gives

$$\Rightarrow e = \overline{\mathbf{D}} \cdot \overline{\mathbf{C}} \cdot \overline{\mathbf{B}} \cdot \overline{\mathbf{A}} + \overline{\mathbf{D}} \cdot \mathbf{B} \cdot \overline{\mathbf{A}} + \mathbf{D} \cdot \overline{\mathbf{C}} \cdot \overline{\mathbf{B}} \cdot \overline{\mathbf{A}}$$

It can be seen that this corresponds to one of the simplifications of the Boolean expression

The Karnaugh map makes these simplifications easier to spot.

Further simplifications are also possible since groupings of "**1**s" can take place by folding around the edges of the map as shown below

The left hand corners can be folded vertically to give the term $\overline{\mathbf{C}} \cdot \overline{\mathbf{B}} \cdot \overline{\mathbf{A}}$.
The top corners can also be folded horizontally to give the term $\overline{\mathbf{D}} \cdot \overline{\mathbf{C}} \cdot \overline{\mathbf{A}}$ but since both of these "**1**s" are incorporated into other terms, the term $\overline{\mathbf{D}} \cdot \overline{\mathbf{C}} \cdot \overline{\mathbf{A}}$ is redundant.
So therefore

$$\Rightarrow e = \overline{\mathbf{D}} \cdot \mathbf{B} \cdot \overline{\mathbf{A}} + \overline{\mathbf{C}} \cdot \overline{\mathbf{B}} \cdot \overline{\mathbf{A}}$$

which is the same as the original Boolean expression after simplification.

Consider as another example, element **c** of the seven segment array. This element is lit for numbers 0, 1, 3, 4, 5, 6, 7, 8, and 9. The truth table is

D	C	B	A	c
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

and the Karnaugh map becomes

There are several ways in which this can be simplified; one such way is shown below.

Grouping together the "**1**s":- the bottom line yields the term $\mathbf{D} \cdot \overline{\mathbf{C}} \cdot \overline{\mathbf{B}}$

the second line yields the term $\overline{\mathbf{D}} \cdot \mathbf{C}$

the left hand top corner yields the term $\overline{\mathbf{D}} \cdot \overline{\mathbf{B}}$

the third column term yields the term $\overline{\mathbf{D}} \cdot \mathbf{B} \cdot \mathbf{A}$

So therefore

$$\Rightarrow c = D \cdot \overline{C} \cdot \overline{B} + \overline{D} \cdot C + \overline{D} \cdot \overline{B} + \overline{D} \cdot B \cdot A$$

Using Karnaugh maps to simplify Boolean expressions.

In all the following examples **A**, **B**, **C**, and **D** are inputs and **Q** is the output.

Consider the three input example $Q = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot C + \overline{B} \cdot \overline{C}$

This is put into a Karnaugh map as follows:

  a "**1**" is put into the place representing **A = 1**, **B = 1**, **C = 1** i.e. $A \cdot B \cdot C$;

  a "**1**" is put into the place representing **A = 0**, **B = 0**, **C = 1** i.e. $\overline{A} \cdot \overline{B} \cdot C$;

  for the term $\overline{B} \cdot \overline{C}$, the value of **A** is not needed and so "**1**s" are put in each location

  where **B = 0** and **C = 0**, i.e. two places.

$$
\begin{array}{c|c|c|c|c}
 & \multicolumn{4}{l}{\textbf{BA}} \\
\textbf{C} & \textbf{00} & \textbf{01} & \textbf{11} & \textbf{10} \\
\hline
\textbf{0} & 1 & 1 & 0 & 0 \\
\hline
\textbf{1} & 1 & 0 & 1 & 0 \\
\end{array}
$$

Grouping together the "1s" gives

So therefore $Q = \overline{C} \cdot \overline{B} + \overline{B} \cdot \overline{A} + A \cdot B \cdot C$

Consider the example $Q = \overline{D} \cdot \overline{C} \cdot B \cdot A + C \cdot \overline{B} \cdot A + \overline{C} \cdot \overline{A} + \overline{A} \cdot B$

"**1**s" must be inserted into the grid for each term:-

  where **D = 0**, **C = 0**, **B = 1**, **A = 1**;

  where **C = 1**, **B = 0**, **A = 1**, and **D = 0** and **1** i.e. two places,

  where **C = 0**, **A = 0**, and where **D = 0** and **1** and where **B = 0** and **1** i.e. four places,

  where **A = 0**, **B = 1**, and where **D = 0** and **1** and where **C = 0** and **1** i.e. four places.

$$
\begin{array}{c|c|c|c|c}
 & \multicolumn{4}{l}{\textbf{BA}} \\
\textbf{DC} & \textbf{00} & \textbf{01} & \textbf{11} & \textbf{10} \\
\hline
\textbf{00} & 1 & 0 & 1 & 1 \\
\hline
\textbf{01} & 0 & 1 & 0 & 1 \\
\hline
\textbf{11} & 0 & 1 & 0 & 1 \\
\hline
\textbf{10} & 1 & 0 & 0 & 1 \\
\end{array}
$$

Grouping the "1s" gives

So therefore $Q = \overline{C} \cdot \overline{A} + C \cdot \overline{B} \cdot A + \overline{D} \cdot \overline{C} \cdot B + B \cdot \overline{A}$

The operation of Combinational Logic Systems.

As well as being able to translate the specification of an electronic sub-system into a Boolean expression it is also necessary to be able to take a Boolean expression and turn it back into a sub-system specification. This becomes particularly useful when, as an electronics engineer you are called upon to repair an electronic system for which the available documentation is incomplete.

For example, a 7 segment array is programmed to display symbols for the normal numbers from 0 to 9 but some new symbols from 10 to 15. Consider element **e** again. With the new symbols the Boolean expression becomes

$$e = D \cdot C + B \cdot \overline{A} + \overline{C} \cdot \overline{B} \cdot \overline{A} + D \cdot B \cdot A$$

So the problem is to work out for which numbers element **e** is lit. To do this each term in the expression is interpreted in turn.

Term $D \cdot C$ means that element **e** is lit when **D = 1, C = 1** and for all combinations of **B** and **A**. i.e. the numbers 12, 13, 14 and 15.

Term $B \cdot \overline{A}$ means that element **e** is lit when **B = 1, A = 0** and for all combinations of **D** and **C**. i.e. the numbers 2, 6, 10, and 14.

Term $\overline{C} \cdot \overline{B} \cdot \overline{A}$ means that element **e** is lit when **C = 0, B = 0, A = 0** and for all values of **D** i.e. the numbers 0 and 8.

Term $D \cdot B \cdot A$ means that element **e** is lit when **D = 1, B = 1, A = 1** and for all values of **C** i.e. the numbers 11 and 15

Therefore element **e** is lit for the numbers 0, 2, 6, 8, 10, 11, 12, 13, 14, and 15.

11.2   SEQUENTIAL LOGIC SYSTEMS

Apart from the very small transition time for logic signals to pass through a logic gate, any change in the inputs to a combinational logic system are immediately translated through to the output. For simple systems this is desirable but there are many systems where events need to take place sequentially. Such systems therefore need to contain sub-systems that can produce time delays and remember whether operations have occurred.

Bistable Latch

A bistable latch (bistable flip-flop) is a circuit that has two stable states and will remember one bit of information. It forms the basis for static computer memories. The circuit of a bistable latch made from **NAND** gates is shown in the diagram alongside.
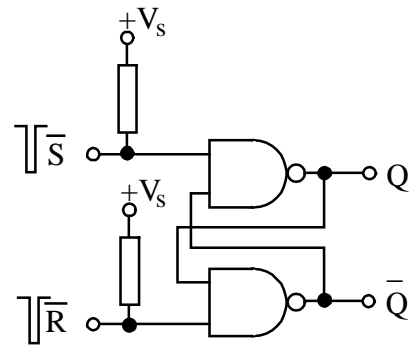
Assume that the **Q** output is **0** and the $\overline{\textbf{Q}}$ output is **1**. It is worth checking that this state is stable. When a short pulse to 0V is applied to the **S** (SET) input, the **Q** output becomes **1** and the $\overline{\textbf{Q}}$ becomes **0**. It is again worth checking that this state is also stable.

If a short pulse to 0V is now applied to the **R** (RESET) input, then **Q** becomes 0 and $\overline{\textbf{Q}}$ becomes 1, i.e. the initial state.

The two resistors act as 'pull-up' resistors and keep the **S** and **R** inputs at logic 1 and it is known as a bistable flip-flop because it has two stable states.

D-Type Flip-Flops.

While the simple bistable flip-flop shown above will remember whether an event has occurred it is impossible to synchronise several of these circuits together. The simple bistable flip-flop also has an unstable state corresponding to the condition when both **S** and **R = 0**. In order to overcome these difficulties a more complex circuit is used which is known as a D-type flip-flop (Data-type flip-flop). Fortunately these circuits are fabricated as ICs and so do not need to be constructed. The circuit symbol for a D-type flip-flop is shown below together with its truth table.
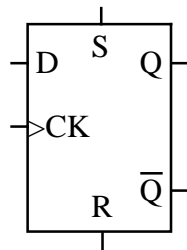
CK	D	Q	$\overline{\text{Q}}$
0	0	Q	$\overline{\text{Q}}$
0	1	Q	$\overline{\text{Q}}$
↑	0	0	1
↑	1	1	0

D is the **Data** input and it is the information on this input that is stored in the flip-flop.

CK is the **Clock** input and it is the state of this input that determines when the information on the Data input is stored in the flip-flop.

**Q** is the output and $\overline{\textbf{Q}}$ is the inverse of **Q**.

S is the **SET** input and makes the output **Q** logic **1** when it is a logic **1** irrespective of the state of **D** and **CK**..

R is the **RESET** input and makes the output **Q** logic **0** when it is a logic **1** irrespective of the state of **D** and **CK**..

The > symbol in front of the **CK** shows that the information on **D** is stored in the flip-flop when the clock input goes from **0** to **1**. This type of D-type flip-flop is said to be rising edge triggered.

An example of such a device is the 4013 IC.

An important use of a D-type flip-flop is as a Data latch for the output from a microprocessor system. The diagram below shows how four D-type flip-flops would be arranged to store the output from a microprocessor system which is written to the four least significant bits of the data bus (D_3, D_2, D_1, D_0).
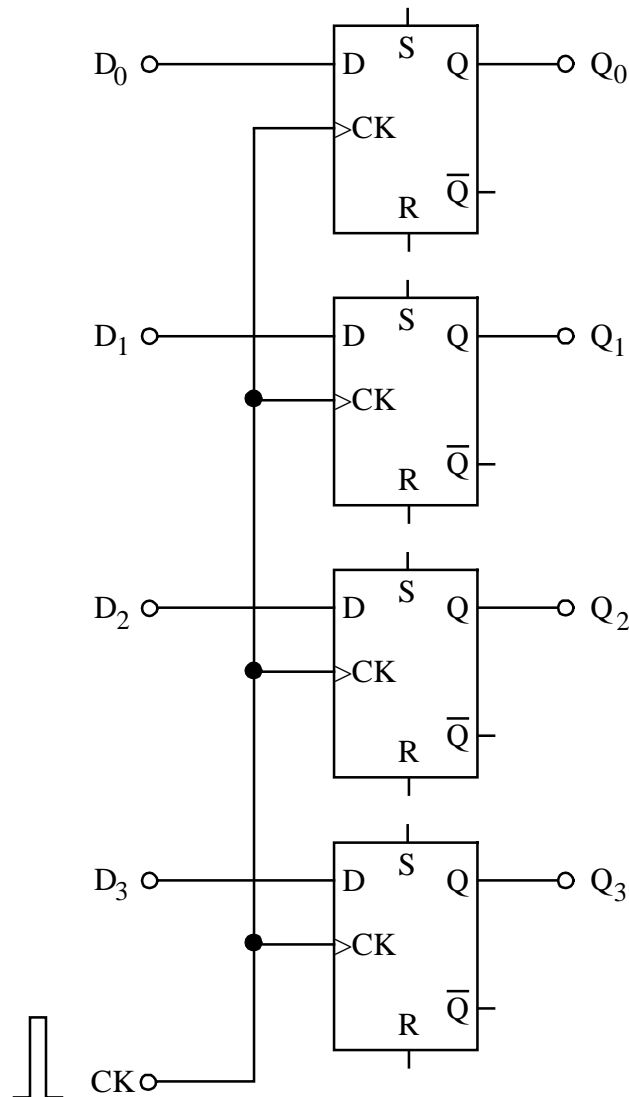
The microprocessor would set up the information to be stored in the latch on D_3, D_2, D_1, D_0 and would then apply a positive going pulse to the clock input. All four D-type flip-flops would then store the data on the rising edge of the pulse. This data would then appear on the outputs Q_3, Q_2, Q_1, Q_0. For this application all the **S** and **R** inputs are connected to logic **0**.

Shift Registers

A shift register is a device that enables data to be passed from one flip-flop to the next, on each successive clock pulse. The very first electronic computer memories were based on this principle. The main use of shift registers now is for the conversion of serial data to parallel data and vice-versa. The circuit diagram of a four bit shift register, made from rising edge triggered D-type flip-flops is shown below.
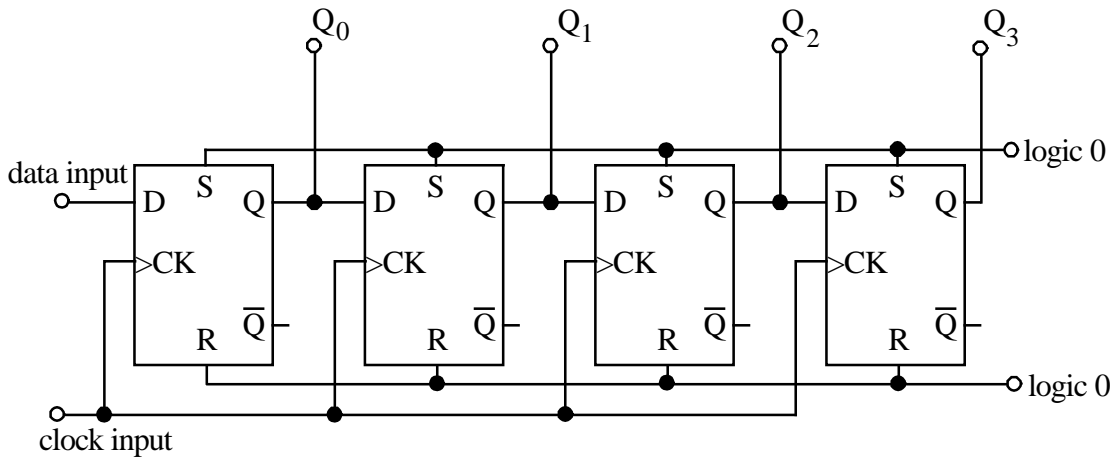
The timing diagram for the shift register is shown below. It assumes that there is a single data input signal of logic **1**, and shows how the data pulse moves from flip-flop to flip-flop on each successive clock pulse.
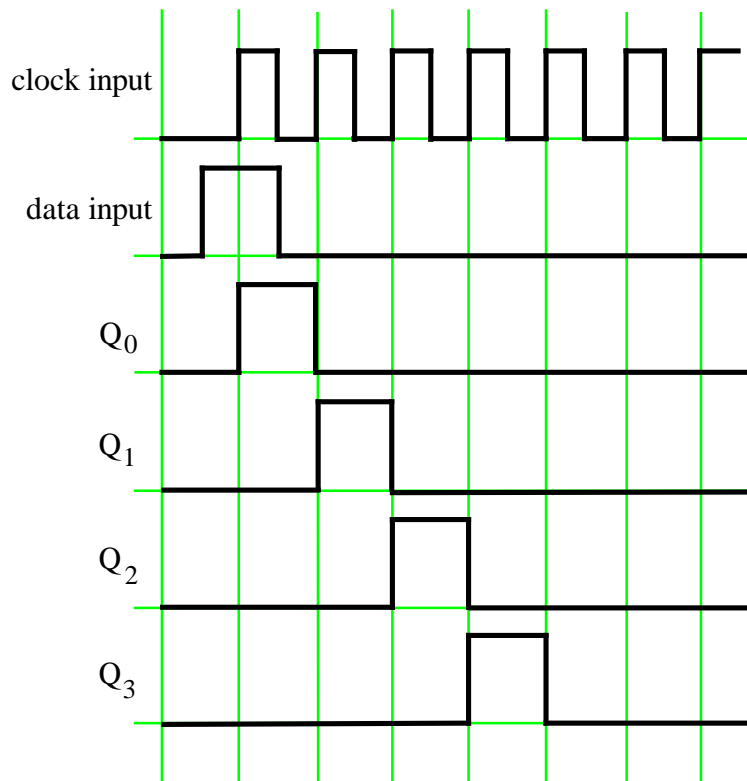
Serial-to-parallel conversion can be accomplished by connecting the serial data input to the **D** input terminal and then reading the parallel data from Q_0 to Q_3 after four clock pulses. For parallel data to be converted to serial data, it is necessary to use the **SET** facility of the flip-flops. This functions in much the same way as the **RESET** input, in that a logic **1** on the **SET** input will set **Q** to logic **1**, a logic **0** having no effect. The parallel input data has to be **AND** gated with a **LOAD** input signal to ensure that the **SET** inputs only receive data at the correct time. The circuit diagram of such a shift register is shown below.
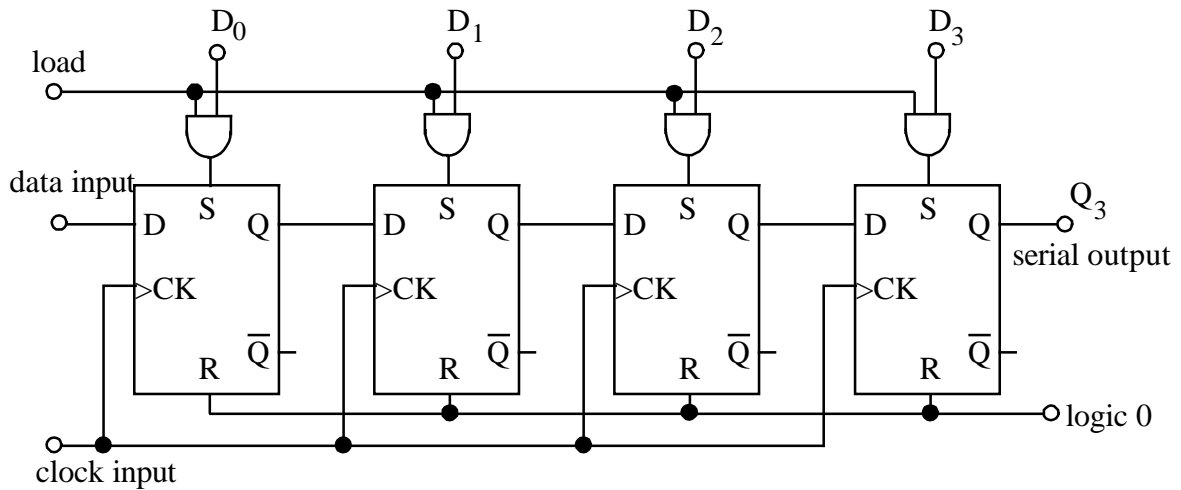
The sequence of operation is as follows:

    a).   A pulse is applied to the **RESET** input to set all of the **Q** outputs to **0**

    b).   The parallel data is set up on the **D** inputs.

    c).   A short pulse to logic **1** is applied to the **LOAD** input.
              This sets the parallel data into the flip-flops.

    d).   Four clock pulses are applied to the **CLOCK** input at the desired data rate, and the serial data is obtained from Q_3.

An interesting application of a large shift register is its use to generate pseudo random numbers by **EX-OR**ing together two of the **Q** outputs and then connecting the output of the **EX-OR** gate to the **DATA** input. For a 17 bit shift register with the **Q** outputs from the **14**th and **17**th **EX-OR**ed together, the sequence length is 131,017 steps before repetition.

The NAND Gate Monostable Circuit.

The 555 monostable circuit has been covered in the support booklet for the Foundation module. Monostables can also be constructed from logic gates, though their timing is not as consistent or as accurate as that of a 555.

The circuit diagram for a monostable using **NAND** gates is shown below.
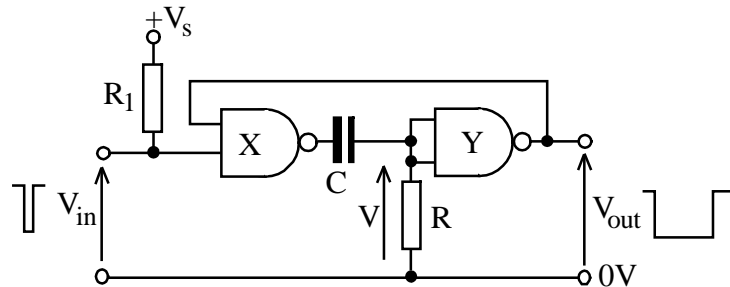
The input voltage, V_{in}, is held at logic **1** by R_1. The inputs of **NAND** gate Y are held at logic **0** by the resistor **R**. Therefore the output, V_{out}, is at logic **1**. Since both inputs of gate X are at logic **1**, the output of X will be at logic **0**. With the capacitor, **C**, discharged this is a stable state. Consider what happen when V_{in} becomes logic **0** for a short time. The output of X will become logic **1** and the supply voltage will appear across **R** as the capacitor begins to charge through **R**. This makes the input to Y logic **1**, so making the output from Y logic **0**. This in turn makes the top input of gate X logic **0** and so will keep the output of gate X at logic **1** even when V_{in} returns to logic **1**.

Meanwhile the capacitor is charging through **R** and as it does, the voltage across **R**, **V**, will decrease. This will continue until **V** is just below the switching threshold of gate Y, i.e. half of the supply voltage. When this happens the output of gate Y will become logic **1**, which in turn will make the top input of gate X logic **1**. With both inputs to gate X now at logic **1**, its output becomes logic **0** and the capacitor discharges as the stable state is again restored.
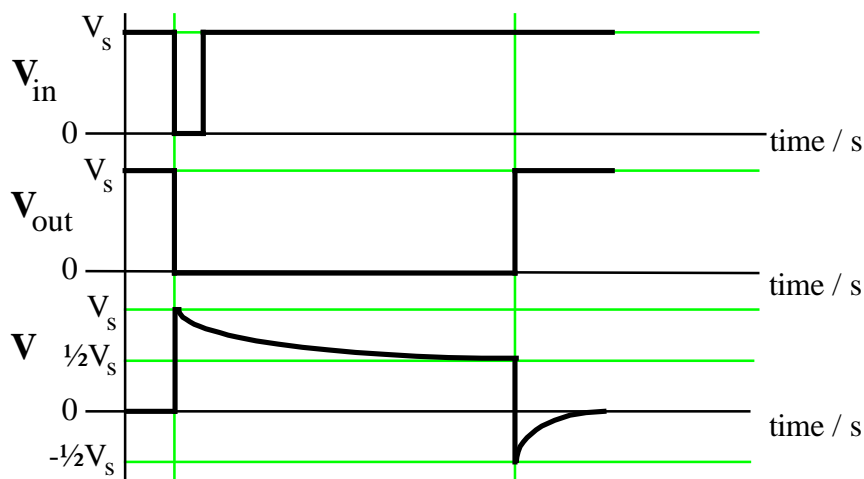
For the monostable to function successfully, the duration of the input pulse must be shorter than the time period of the monostable.

The duration of the output pulse, in seconds, of the monostable is given approximately by

$$T = C\,R$$

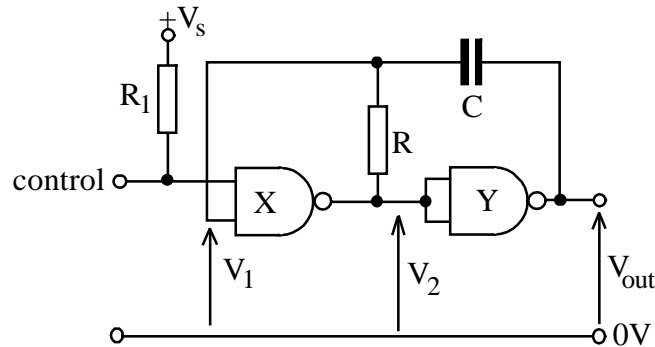where **C** is in farads and **R** is in ohms.

The sketch graphs below show the operation of the monostable.

NAND gate monostables are triggered with 'negative going' pulse, and so are said to be 'falling edge triggered'.

The NAND Gate Astable Circuit.

As well as being able to form monostables, two **NAND** gates can be used to form an astable. The basic circuit is shown below.

When the astable circuit is switched off, the capacitor is discharged. When the circuit is switched on and there is no connection to the control input, imbalances between the two **NAND** gates will ensure that one of the **NAND** gate outputs will become logic **1**. Assume that gate Y's output becomes logic **1**. This means that the input to gate Y must be logic **0**, as must the output of gate X. This in turn means that the input to gate X must be logic **1**, which it will be since the capacitor will be charging through **R** from the output of gate X. So the circuit is semi-stable. As the capacitor charges, V_1 will decrease until it is just less than half of the supply voltage. When this happens, the input to gate X becomes a logic **0** and so the output of gate X will become logic **1**. This in turn makes the input to gate Y logic **1**, so the output of gate Y becomes logic **0**. The voltage that was across the capacitor, as a result of it partly charging, will now be moved **down** by the supply voltage, V_s, so that
$V_1 = -\frac{1}{2}V_s$.
The capacitor will now charge up in the other direction, through **R**, until V_1 is just greater than $+\frac{1}{2}V_s$. When this happens the input of gate X will be a logic **1**, so making its output a logic **0**, which in turn will make the output of gate Y logic **1** again. The capacitor will again have a voltage of $\frac{1}{2}V_s$ across it and so when the output of gate Y becomes logic **1**, the voltage levels of the capacitor will be shifted **up** by V_s so making $V_1 = 1\frac{1}{2}V_s$. The capacitor will now start to discharge through **R** until V_1 falls to just less than $\frac{1}{2}V_s$, and so the whole process repeats. It should be noted that the initial output pulse is shorter than the consequent pulses due to the fact that the capacitor was initially discharged. It should also be noted that since the capacitor has to charge up in both directions, electrolytic capacitors are not suitable for this application. This effectively limits the maximum value of C to $1\mu F$.

To a first approximation, the frequency of oscillation of the astable is given by

$$f = \frac{1}{2RC}$$

It is found in practice that the value of the supply voltage and the ambient temperature affect the frequency of operation.

The sketch graphs below show the operation of the astable when there is no connection made to the control input.
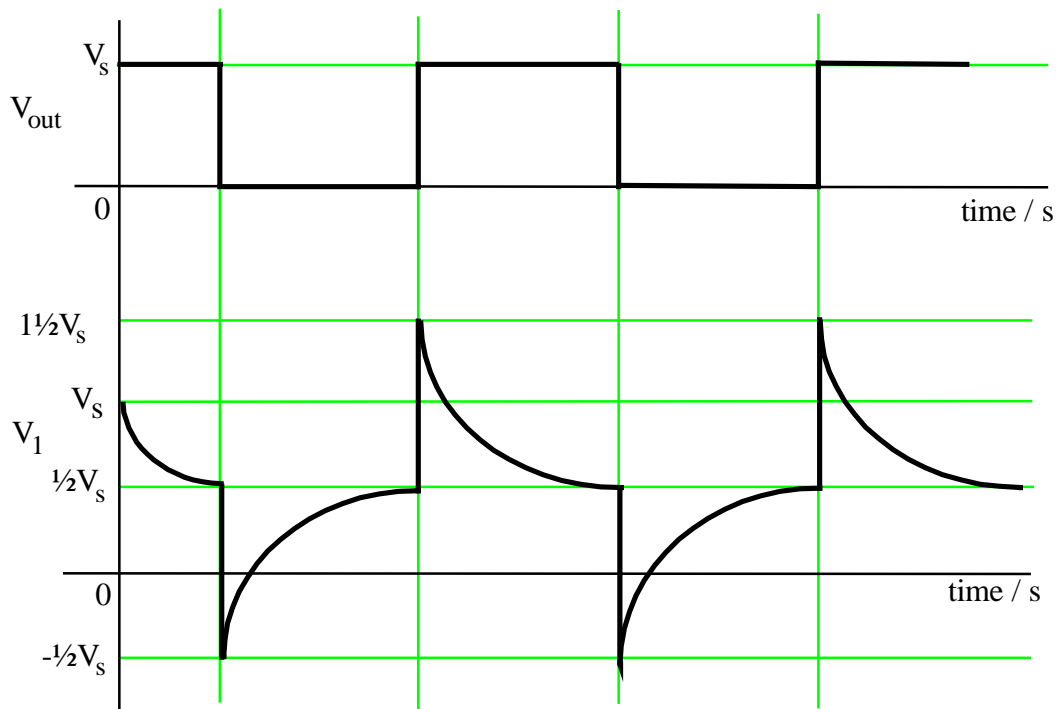
The control input provides a convenient way to stop and start a **NAND** gate astable. If the control input is at logic **1** the astable operates normally. If the control input is at logic **0** then the output of gate X becomes logic **1** so making the output from gate Y logic **0** and so stopping the oscillation. The resistor R_1 is a 'pull up' resistor so that if nothing is connected to the control input then it will be held at logic **1**. If the control facility is not required, R_1 can be omitted and the two inputs of NAND gate X connected together.

11.3 COUNTERS

To enable a D-type flip-flop to toggle, i.e. change state on each successive clock pulse, the **D** input should be connected to the $\overline{Q}$ output. The **D** input is then always opposite to **Q** and so toggling occurs on each successive clock pulse. The arrangement is shown below, where the D-type flip-flop is shown with its normal logic symbol.
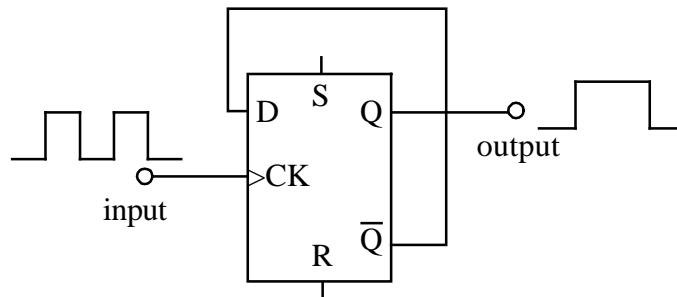
Both the **SET** and **RESET** inputs are connected to logic **0**.
This circuit has many applications since it effectively has an output frequency that is half the input frequency. The circuits can also be combined together to form binary counters.

Binary, Decimal and Hexadecimal Numbers

The number system that is in common everyday use is founded on ten different numbers:-

$$0, \ 1, \ 2, \ 3, \ 4, \ 5, \ 6, \ 7, \ 8, \ 9$$

This number system is known as the **DECIMAL** or **DENARY** system. (Denary means 10).
These numbers on their own are called **UNIT**(s) and enable numbers in the range 0 to 9 to be represented.
For numbers that are larger than 9 a second column of numbers is needed.
This second column is called the **TEN**(s) column. So 9+1 would be represented by putting a 1 in the tens column and a 0 in the units column eg.

10

For 9+2, a one is put in the tens column and the one unit left over is put into the units column, e.g.

11

For 9+5, ten is subtracted and a 1 is put in the tens column. This leaves 4 units and so a 4 is put in the units column, e.g.

14

In this way numbers up to 99 can be represented. For numbers greater than this another column is needed to represent 99+1 i.e. the **HUNDRED**(s). So for 99+1, a 1 is put in the hundreds column. This would leave no tens and no units, so a 0 is put in the tens column, and a 0 in the units column, e.g.

100

For the number given by 99+5 a 1 is put in the hundreds column, leaving no tens and four units and so 99+5 is written as

$$104$$

In this way numbers up to 999 can be represented. Beyond this another column needs to be introduced. This is called the **THOUSAND**(s) column, etc.

The units column represents single numbers
$$\text{i.e. } \mathbf{n \times 1 \ (n \times 10^0)}$$
where n is any number between 0 and 9.
The tens column represents numbers multiplied by ten
$$\text{i.e. } \mathbf{n \times 10 \ (n \times 10^1)}$$
where n is any number between 0 and 9.
The hundreds column represents numbers multiplied by 100 (10×10),
$$\text{i.e. } \mathbf{n \times 10 \times 10 \ (n \times 10^2)}$$
The thousands column represents numbers multiplied by 1000 ($10 \times 10 \times 10$),
$$\text{i.e. } \mathbf{n \times 10 \times 10 \times 10 \ (n \times 10^3)}$$
And so on.

Computers are very basic machines compared to even the most innumerate human.
Computers, since they work using digital electrical circuits, only have two states; ON which is represented by a **1** and OFF which is represented by a **0**. Such a number system is called **BINARY**.
This means that a computer can only count to 1 before it needs to introduce another column, the **TWO**s column (compare with the *tens* column in decimal).
So for 1 + 1 a 1 is put in the twos column, leaving a 0 in the units column,

$$\text{i.e. } \quad 1 + 1 = 10$$

Therefore $$1 + 1 + 1 = 11$$

But for the next number it is necessary to introduce another column, the **FOUR**s column so that
$$1 + 1 + 1 + 1 = 100$$

(Compare this with the *hundreds* column in decimal.)
The next column to introduce is the **EIGHT**s column.
It should be clear that each time it is necessary to introduce another column it is multiplied by two again. (Compare this with the way in which each new column was multiplied by ten in the decimal system.).
So in the binary system the columns are:

UNITs	(2^0)
TWOs	(2^1)
FOURs	(2^2)
EIGHTs	(2^3)
SIXTEENs	(2^4)
THIRTY TWOs	(2^5)
etc.	

Addition, subtraction, multiplication and division are all done in the same way as in the decimal system except that the largest number in any column is 1.

As computers have become faster, they now treat the columns of the binary system in blocks of four. This means that they now count in SIXTEENs instead of TWOs. Such a number system is known as **HEXADECIMAL**.

This means that it is necessary to represent numbers larger than 9 as a single character and the characters that are used are the first six letters of the alphabet, i.e. A, B, C, D, E and F

DECIMAL   1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HEXADECIMAL   1 2 3 4 5 6 7 8 9 A B C D E F

Using this system, numbers up to fifteen can be represented in the units column. The next column is the **SIXTEEN**s column and so the decimal number 16 would be written as

10

in hexadecimal. (Compare this to the *tens* column in the decimal system).

The third column in the Hexadecimal system is the 16x16 column or the **TWO-HUNDRED-AND-FIFTY-SIX** column.

In Module 3 it will be necessary to be able to convert large numbers between binary, decimal and hexadecimal. This module only requires such conversions up to and including the number 15. The easiest way of converting such numbers is by using a conversion table as shown below.

DECIMAL	BINARY	HEXADECIMAL
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

4-Bit Up or Down Counters

D-type flip-flops that are wired to toggle can be cascaded together to produce a BINARY Counter. Four such flip-flops are shown below connected together as an ASYNCHRONOUS counter. All of the flip-flops considered are rising edge triggered.
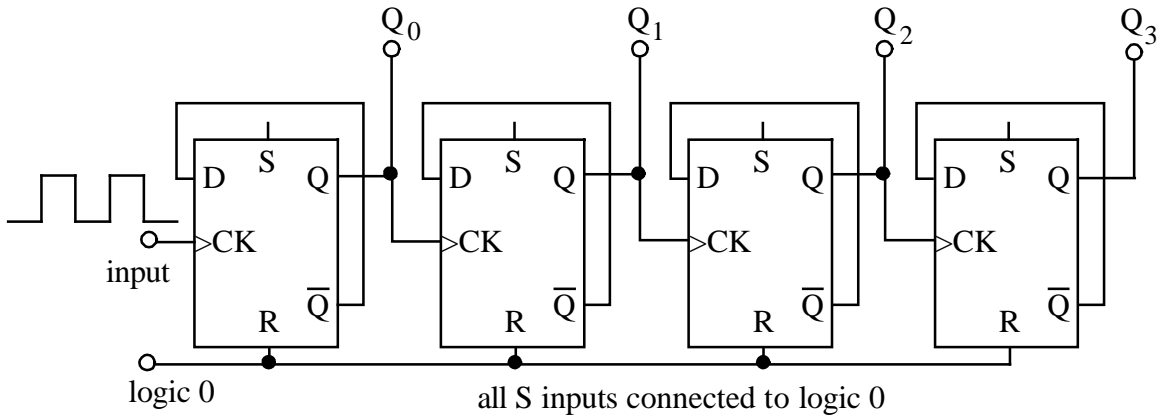

The waveforms obtained from each of the **Q** outputs can be seen in the timing diagrams below. Note how the circuit counts down in binary, the decimal numbers being included at the bottom of the figure as a guide. The counter counts down from 15 and resets back to 0, the process then repeating. This circuit is a '**down counter**'.
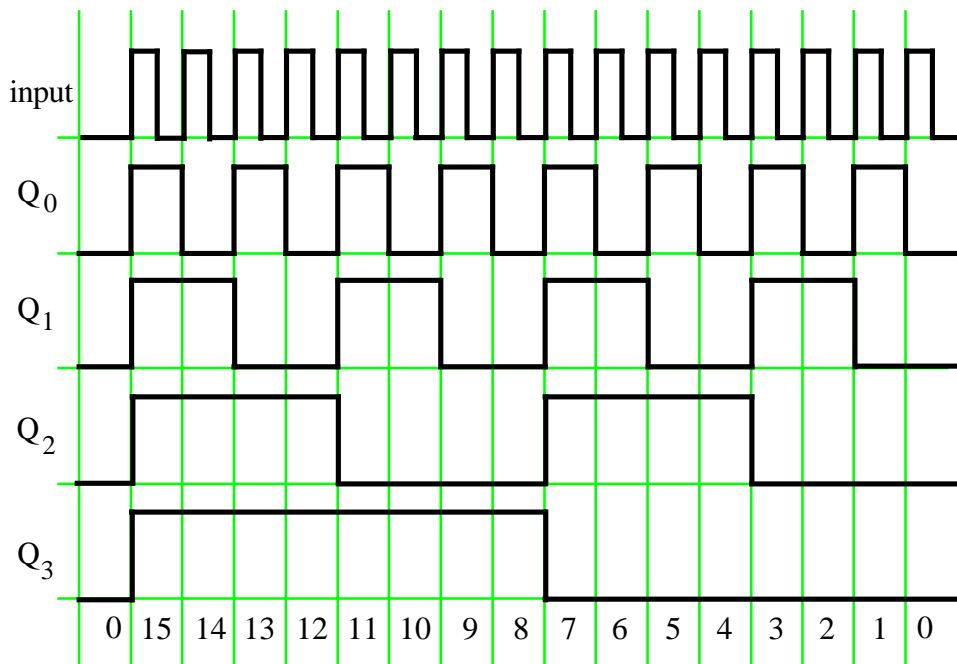

It should also be noted that the Binary counter circuit will also act as a frequency divider, with Q_0 being half the frequency of the input, Q_1 being half the frequency of Q_0 and so on.

To make a binary **up counter** it is necessary to connect each successive clock input to the preceding $\overline{Q}$ output as shown in the next diagram.
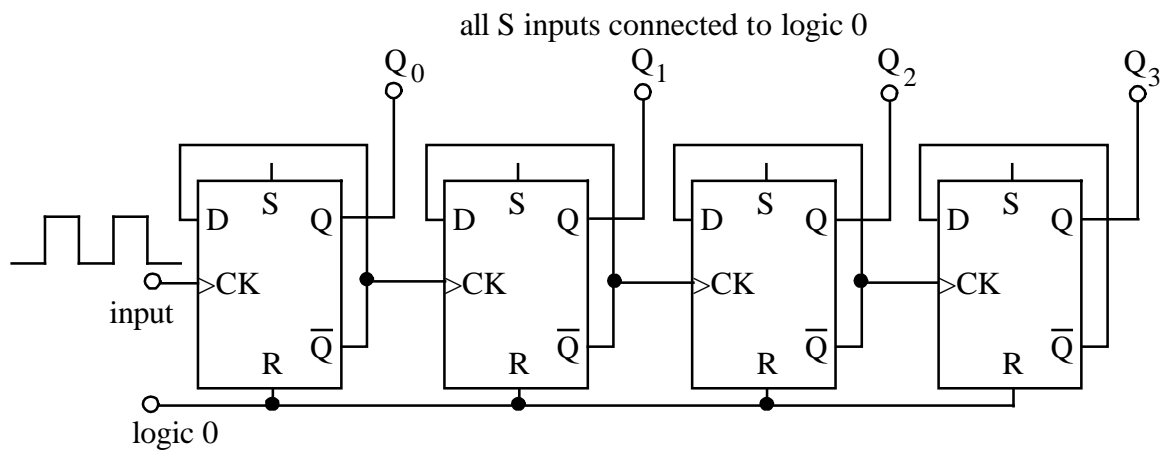
The corresponding timing diagrams showing the **Q** outputs are shown below.
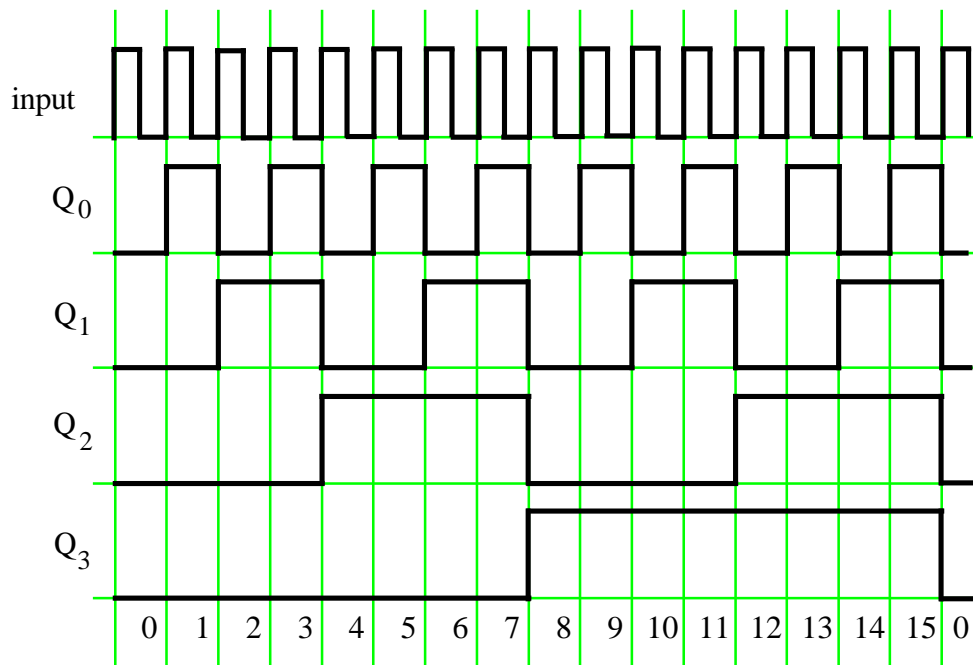
This time the circuit counts upwards, the decimal numbers being included at the bottom of the diagrams as a guide.

Often a counter is required that counts up to a number other than 15 before resetting itself. The most common is the Binary Coded Decimal (**BCD**) counter which counts up to 9 and then resets. This is achieved by **AND** gating together the Q_1 and Q_3 outputs. When both of these are at logic **1**, i.e. on the 10th input pulse, the output from the **AND** gate is used to **RESET** all the flip-flops. The circuit diagram of such a counter is shown below together with the waveform timing diagrams.

all S inputs connected to logic 0
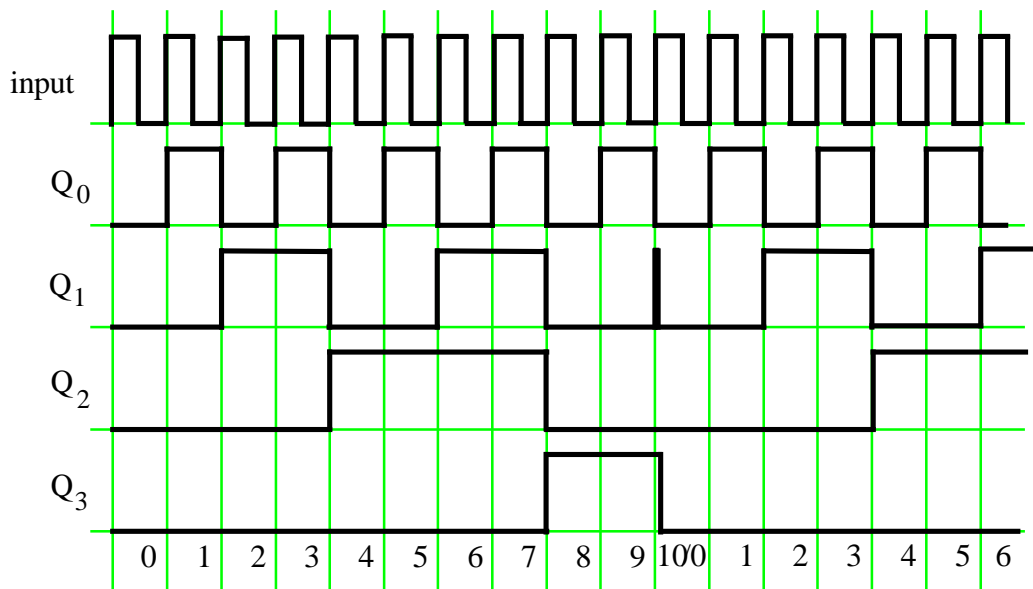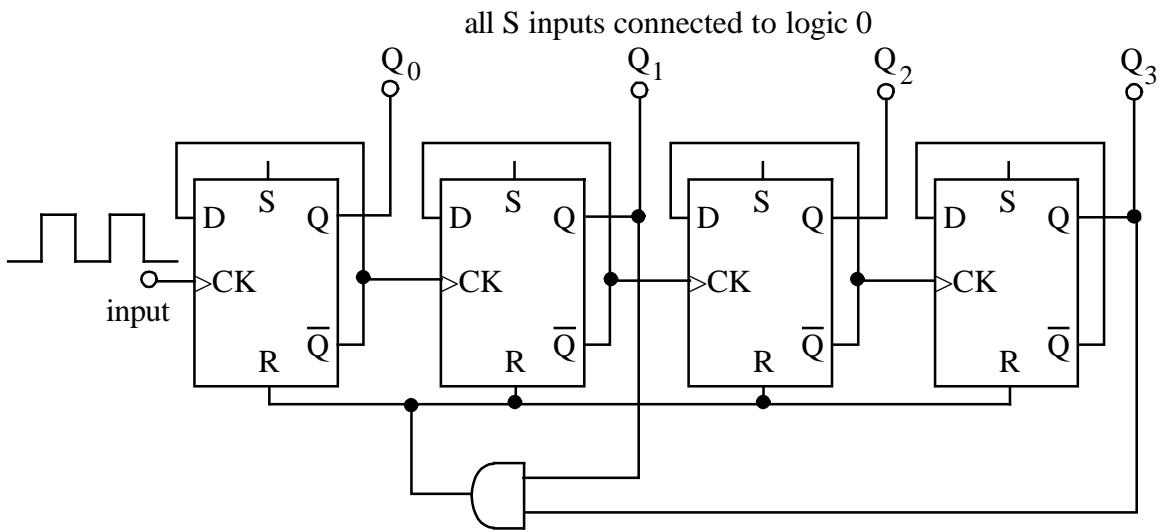
This circuit can also be used to frequency divide the input by ten. However, the output waveform from Q_3 does not have a **mark to space ratio** of 1:1. If a symmetrical output is required from a divide by ten counter then it is necessary to separate the circuit into a divide by five circuit followed by a divide by two circuit.

Such an arrangement is shown below together with the waveform timing diagram.

all S inputs connected to logic 0
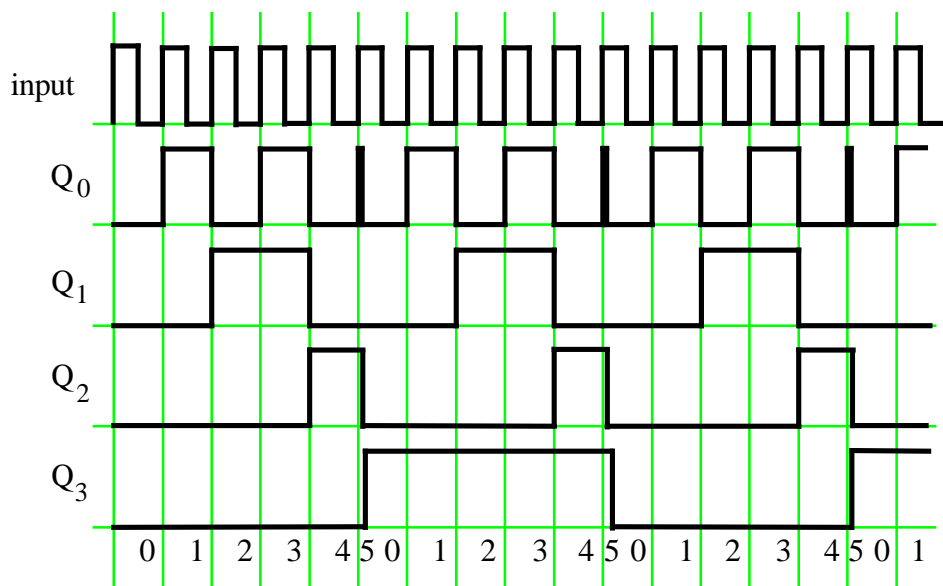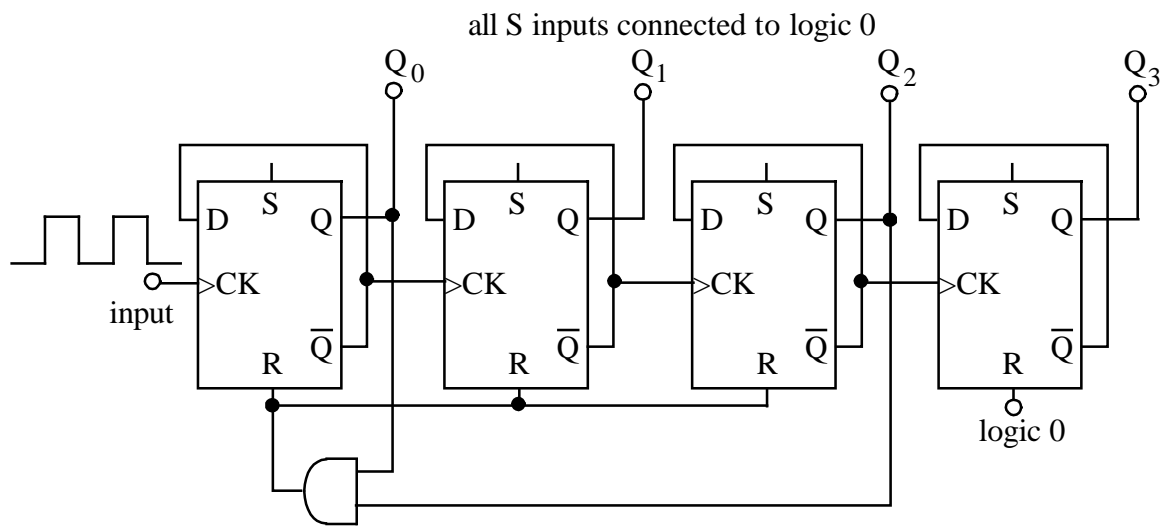
The same principles can also be applied to any even numbered binary counter / frequency divider.

Unfortunately there is a serious problem that occurs with asynchronous counters operating at high frequency which originates from the fact that there is a finite time delay between a clock input pulse going high and the Q output responding. This is called the *propagation delay* and for the 74HC series of counters is typically 20ns. While this is a short time for one counter it becomes very noticeable for long chains of counters operating at a high frequency.

Consider a chain of 12 flip-flops arranged as an asynchronous counter, each with a propagation delay of 20ns. Now, before the last flip-flop can change state, the one before must change as must the one before and so on. So for the situation where all the counters are going to change state, the difference in time between the first and last flip-flop changing will be 240ns. If the frequency of the input signal is 4MHz (period 250ns), the last flip-flop will be changing state almost one complete clock cycle after the first flip-flop. This could cause very serious problems if the last flip-flop's output was being gated with an output from a flip-flop near the beginning of the chain. The problem can be overcome by using *synchronous counters* in which all of the flip-flops are clocked together, but a knowledge of this is not required in this specification.

Using 7-segment arrays with BCD and Hexadecimal counters.

The decoding of binary and hexadecimal numbers for use with a 7-segment array has already been considered in the first section of this booklet. The use of simple logic gates is prohibitively complex for this task, but fortunately there are several ICs available that will take a binary, BCD or hexadecimal input and decode it to operate a 7-segment array directly.

The most common 7-segment decoder is the 4511 IC and apart from the decoder it also contains a four bit latch so as to remember the number that is being decoded. For numbers greater than 9 the display is blanked.
An old 7-segment decoder IC is the 7447. This does not contain a latch but does display symbols when the input number is greater than 9. Unfortunately the symbols displayed are not the standard hexadecimal symbols.
The 4026 and 4033 IC not only contain 7-segment array decoders; they also contain decade counters as well. Again they do not display symbols for inputs greater than 9.

The options available to produce a full hexadecimal display on a 7-segment array include:
a).   designing one's own using Karnaugh maps, Boolean algebra and logic gate ICs,
b).   programming a Programmable Interface Controller IC (PIC) to form the display,
c).   using an EPROM, by programming into it the required outputs,
d).   using a programmable Logic Array (PAL) in a similar way to an EPROM.

Some of these techniques will be considered in Module 3.

11.4 OPERATIONAL AMPLIFIERS

The general properties of operational amplifiers were discussed in the chapter for the Foundation module. This section extends the use of op-amps beyond comparators to their use as voltage amplifiers.

General Amplifier Definitions

An amplifier is designed to produce an output voltage or current which is an enlarged copy of the input voltage or current. When power amplification occurs the extra power is provided by the external power supply. The peak power output is limited by the power supply voltage. The gain is calculated by the ratio of the output quantity to the input quantity.

$$\text{voltage gain} = \frac{\text{output voltage } (V_{out})}{\text{input voltage } (V_{in})}$$

$$\text{power gain} = \frac{\text{output power } (P_{out})}{\text{input power } (P_{in})}$$

Bandwidth.

The bandwidth of an amplifier is the range of frequencies within which the power gain does not fall below **half** of its maximum value. Since

$$\text{power} = \frac{V^2}{R}$$

the bandwidth is also the range of frequencies within which the voltage gain does not fall below $1/\sqrt{2}$ (i.e. 0.7) of its maximum value.

The gain of a capacitor coupled amplifier decreases at the lower frequencies due to the increasing reactance of the capacitors, and at the upper frequencies due to stray capacitance in the circuit.

A typical **voltage gain - frequency** curve is shown below. The frequency is plotted on a log scale to accommodate the large range.
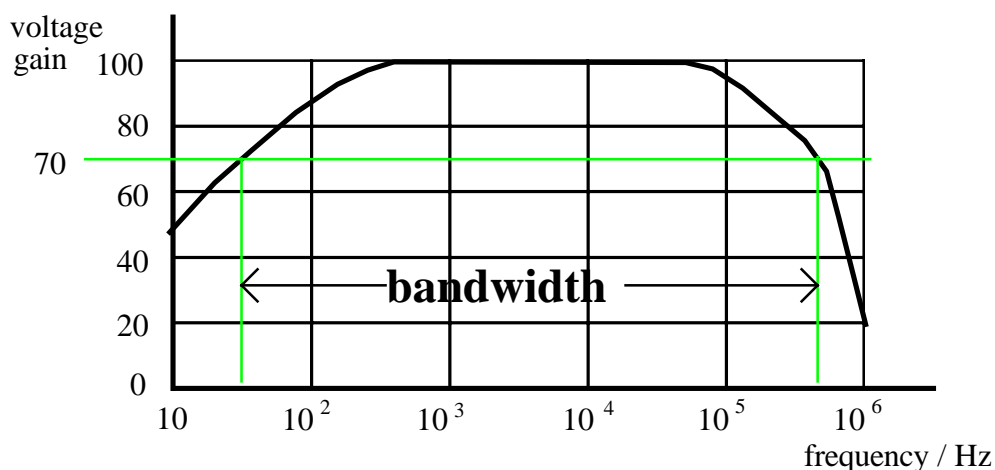
Most op-amps have very large voltage gains, often as high as 10^6. Such large voltage gains require considerable care to be taken if the circuit is to be stable and not prone to oscillation. It is essential for the output terminals to be well separated from the input terminals to prevent positive feedback occurring through stray capacitance. To help ensure that an op-amp is stable a small capacitor is connected between the output terminal and the inverting input terminal. The effect of this is to make the voltage gain of the op-amp decrease with increasing frequency. Consider an op-amp with an open loop voltage gain of 10^6. The graph below shows how the open loop voltage gain varies with frequency.
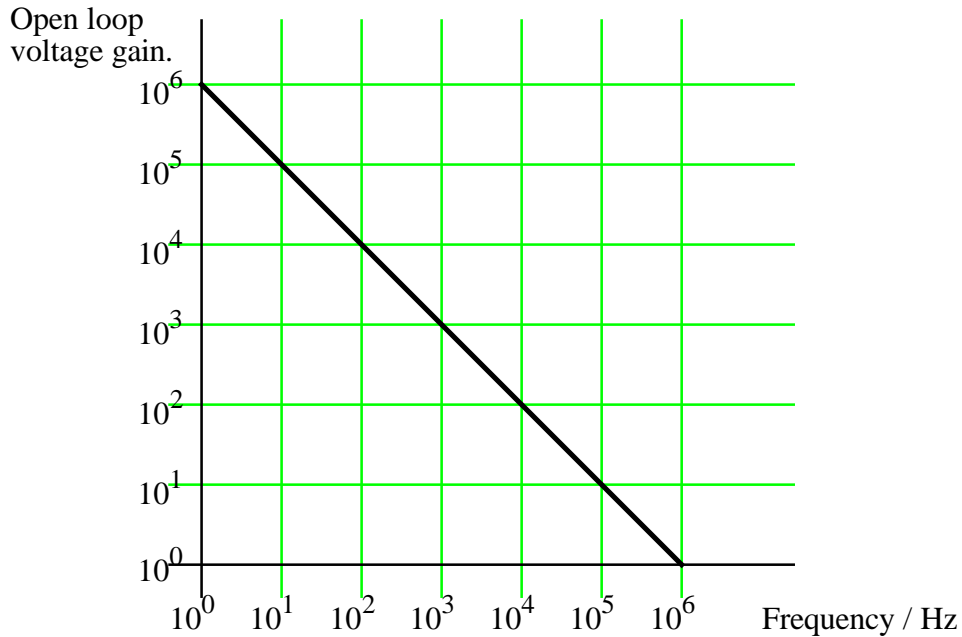
As can be seen from the graph, the voltage gain decreases with frequency so that at a frequency of 1MHz, the voltage gain has fallen to 1. This can be summarised by the formula

**voltage gain × bandwidth = constant**

In the case of the example given above the constant is 10^6.
Using such frequency compensated op-amps it is therefore not possible to have a single op-amp circuit with a large voltage gain and a large bandwidth. Therefore in order to produce amplifiers with large voltage gains and large bandwidths it is necessary to use several low gain op-amp circuits cascaded together.

11.5 INVERTING AMPLIFIER

For most amplifiers, the open-loop voltage gain of an op-amp is too large to be of practical use. Since it is not possible to adjust the open loop gain of an op-amp, to enable them to be used in normal amplifier circuits, **Negative Feedback** is used to reduce the overall gain of the circuit. With negative feedback a proportion of the output signal is 'fed-back' to the input with a phase shift of 180°. This has the effect of cancelling out part of the input signal and so reduces the apparent gain of the whole circuit. With an op-amp, negative feedback is the only way of controlling the voltage gain of the circuit. The voltage gain of the op-amp itself is unchanged but the overall voltage gain of the circuit is reduced significantly. The simplest example of this is the **Inverting Amplifier**.

The circuit diagram of an inverting amplifier is shown below. The power supply connections are not shown, but it is assumed that the circuit is operating from a dual voltage power-supply.
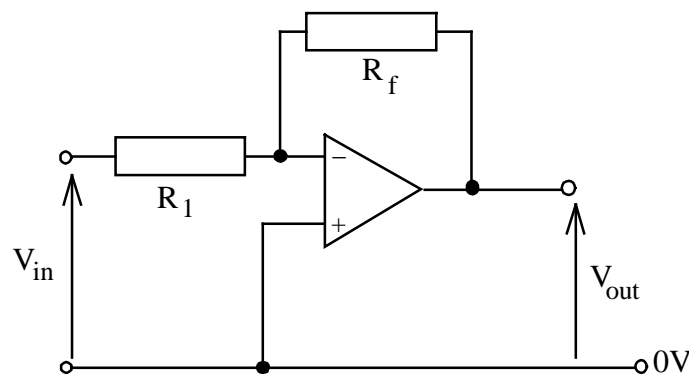
Since it is assumed that the open loop gain of the op-amp is very large, if the output voltage is to be less than the power supply voltage then the difference in voltage between the two input terminals will be very small. The positive input terminal is connected to 0V and so the negative input terminal will be virtually at 0V, i.e. it is a **Virtual Earth point**. The input voltage, V_{in}, appears across the resistor R_1, so a current of V_{in} / R_1 passes through R_1. This therefore makes the input resistance of the circuit equal to R_1. It is assumed that the input impedance of the op-amp is so large that no current passes into its input terminals. Therefore the only path for the current passing through R_1 is through R_f. As the negative input terminal of the op-amp is at virtual earth, the output voltage V_{out} appears across the resistor R_f. This causes a current of V_{out} / R_f to pass through R_f.

$$\frac{V_{in}}{R_1} = -\frac{V_{out}}{R_f}$$

Rearranging gives

$$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1}$$

Therefore the voltage gain of the inverting amplifier is determined solely by the two external resistors; the negative sign indicating that the amplifier is inverting.

It should be noted that the voltage gain of the op-amp has not been altered; it is still very large at low frequencies. But the voltage gain of the overall circuit (closed-loop gain) has been reduced significantly. Also it is important to realise that the equation is only valid when the open-loop gain is significantly greater than the voltage gain of the whole circuit. At high frequencies the voltage gain of the whole circuit will decrease in line with the frequency compensation of the op-amp itself. The bandwidth of the amplifier will depend on the product

of the closed-loop gain of the circuit and the bandwidth. For the purpose of this syllabus, the product of voltage gain and bandwidth is assumed to be 10^6

i.e. **voltage gain $\times$ bandwidth $= 10^6$**

So for an amplifier with a closed-loop voltage gain of 100, the bandwidth will be 10kHz. This, and other examples are shown in the diagram below.
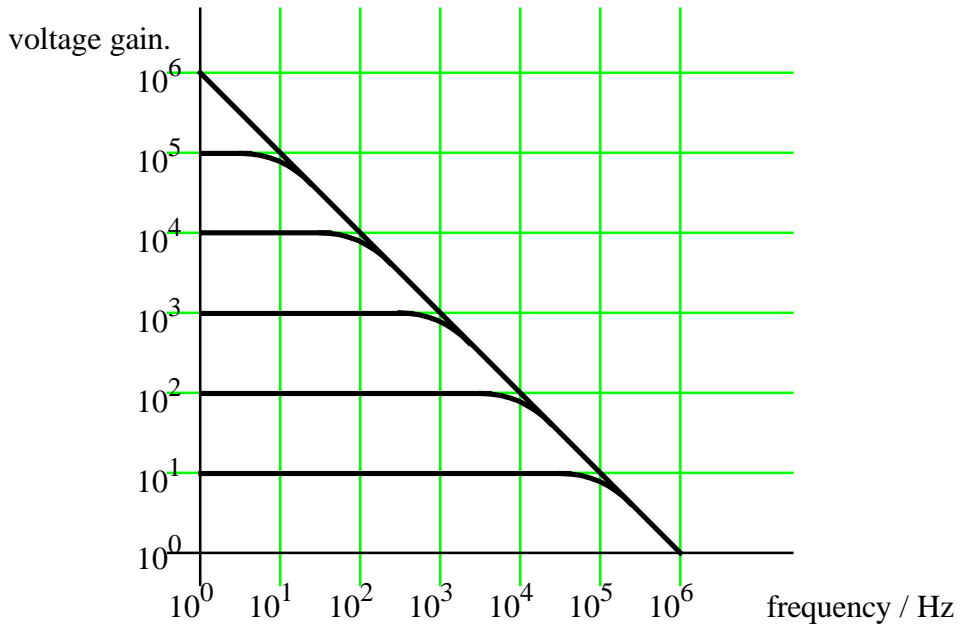
The oscilloscope screen diagram below shows the input and output waveform for an inverting amplifier with a voltage gain of four. As can be seen, the output waveform is four times as large as the input waveform and the output waveform is inverted (out of phase by 180º) compared to the input signal.
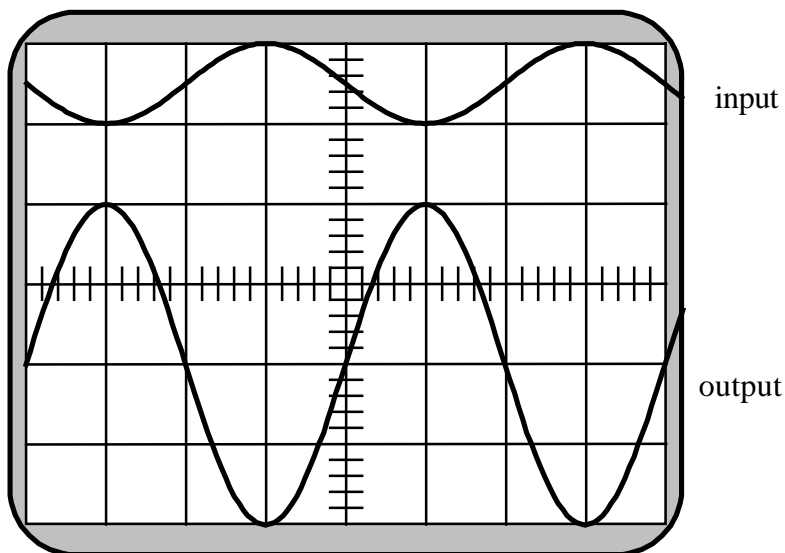
11.6   NON-INVERTING AMPLIFIER

The circuit diagram of a non-inverting amplifier is shown below. The circuit uses negative feedback to reduce the overall voltage gain of the circuit, but the input signal is connected to the positive input of the op-amp. This has the advantage of providing 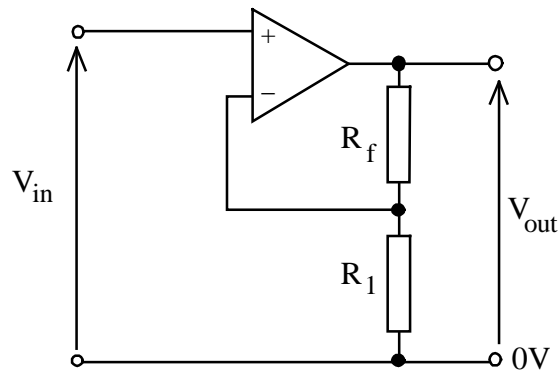an input impedance for the circuit equal to the input impedance of the op-amp itself, which can be as high as $10^{12}\Omega$.

When considering the voltage gain of this circuit it is important to remember that the output voltage of an op-amp is equal to the differential input voltage multiplied by the open loop voltage gain. Since the open loop gain of the op-amp is very large at low frequencies, the voltage at the positive input terminal and the voltage at the negative input terminal of the op-amp will be almost identical, so long as the output has not saturated at the power supply voltage. The voltage at the negative input terminal of the op-amp will be the same as that of the junction of the two resistors $\mathbf{R_f}$ and $\mathbf{R_1}$ and will equal:

$$\frac{\mathbf{V_{out}} \times \mathbf{R_1}}{(\mathbf{R_f} + \mathbf{R_1})}$$

But this will also be equal to the input voltage $\mathbf{V_{in}}$ since the two op-amp input terminals must have almost the same voltage, if the op-amp is not to saturate.

$$\Rightarrow \mathbf{V_{in}} = \frac{\mathbf{V_{out}} \times \mathbf{R_1}}{(\mathbf{R_f} + \mathbf{R_1})}$$

$$\Rightarrow \frac{\mathbf{V_{out}}}{\mathbf{V_{in}}} = \frac{(\mathbf{R_f} + \mathbf{R_1})}{\mathbf{R_1}} = 1 + \frac{\mathbf{R_f}}{\mathbf{R_1}}$$

The non-inverting amplifier has the same limitations at high frequencies as the inverting amplifier owing to the frequency compensation of the op-amp, but it does have the advantage of having a very large input impedance.

The Voltage Follower

The circuit diagram of a voltage follower is shown below and should be thought of as a special case of a non-inverting amplifier, where R_f has a value of zero ohms and R_1 has an infinitely large value.
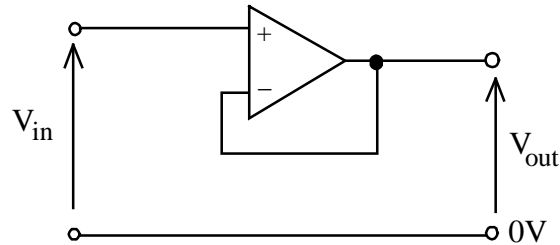
The equation for the non-inverting amplifier then simplifies to

$$\frac{V_{out}}{V_{in}} = 1$$

i.e. the output voltage 'follows' the input voltage. This circuit is used as a buffer amplifier and has a very large input impedance and a low output impedance. So although it has a voltage gain of 1, it does have considerable current and power gain and can very effectively isolate a source from a load.

Practical applications for the voltage follower include:
a)   Increasing the input resistance of a moving coil meter so that the meter does not affect the measurements in any circuit that it is connected to.
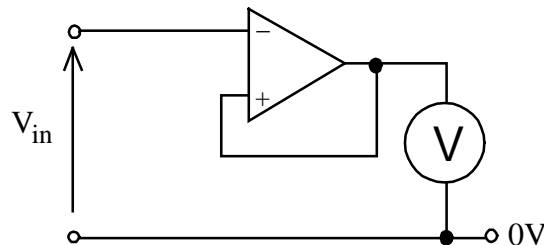
b)   A charge meter, so that electric charge can be measured. With a 1μF capacitor connected as shown, the reading on the meter, in volts, is equal to the charge stored in the capacitor, in microcoulombs.
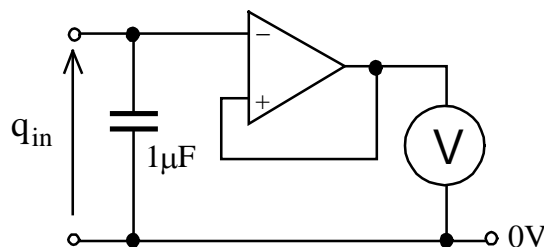
This circuit can also be used as a 'sample and hold' circuit by placing an electronic switch in series with the input.

Feedback.

Feedback occurs when a portion of the output is allowed back into the input. This can occur in **two** ways; it can cancel out part of the input signal and so is called **Negative Feedback**, or it can reinforce the input signal and so is called **Positive Feedback**.

Negative Feedback.
This is when a proportion of the output signal is 'fed-back' to the input with a phase shift of 180°. This has the effect of cancelling out part of the input signal and so reduces the apparent gain of the whole circuit.
The use of negative feedback has already been considered in the inverting and non-inverting op-amp amplifier circuits in order to reduce the voltage gain of the circuit to the required amount. In doing so, it also has the advantage of increasing the bandwidth of the circuit and reducing any distortion that may be introduced by the amplifier.

Positive Feedback.
This is when a proportion of the output signal is 'fed-back' to the input with a phase shift of 0°, i.e. in phase with the input signal. This has the effect of increasing the input signal and so increasing the apparent gain of the whole circuit. All oscillator and astable circuits rely on positive feedback to make them unstable and oscillate. The **NAND** gate bistable latch uses positive feedback to force the change of state once it has been triggered. The 'Schmitt trigger circuit', which is studied in Module 3, also uses positive feedback to increase its switching speed.

When constructing amplifiers with a large voltage gain, especially radio frequency amplifiers, it is imperative to ensure that the output circuit is kept as far away as possible from the input circuit. Failure to do so will almost certainly lead the amplifier system to be unstable at certain frequencies or in the worst case, oscillate very strongly at a particular frequency and be completely uncontrollable.
A good indication of the stability of an amplifier is to measure its voltage gain for a range of frequencies. Any unexplainable increase in voltage gain at a particular frequency is a good indication that the system is not as stable as it should be.

11.7   SUMMING AMPLIFIER

This is a variation of the inverting amplifier, where, instead of there being one input resistor there are several. The circuit diagram of a summing amplifier is shown below.
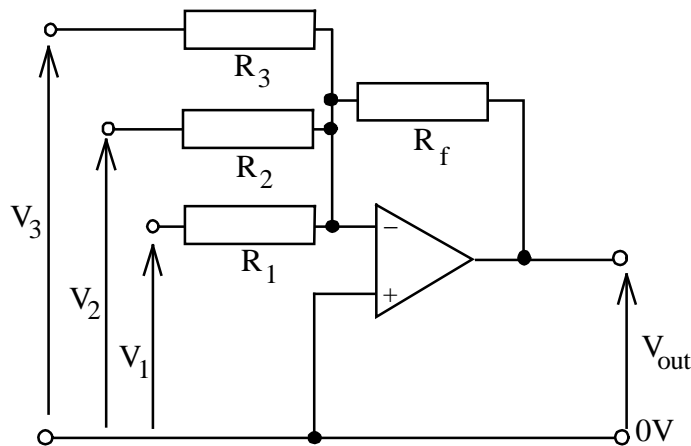
As with the inverting amplifier, the negative input terminal of the op-amp is a virtual earth point and so the current at this point is the sum of the currents passing through the individual input resistors, i.e. the total current is

$$I = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

and this current must be equal to the current passing through R_f as a result of V_{out},

$$\text{i.e.} \quad I = \frac{V_{out}}{R_f}$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_{out}}{R_f}$$

$$\Rightarrow V_{out} = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$
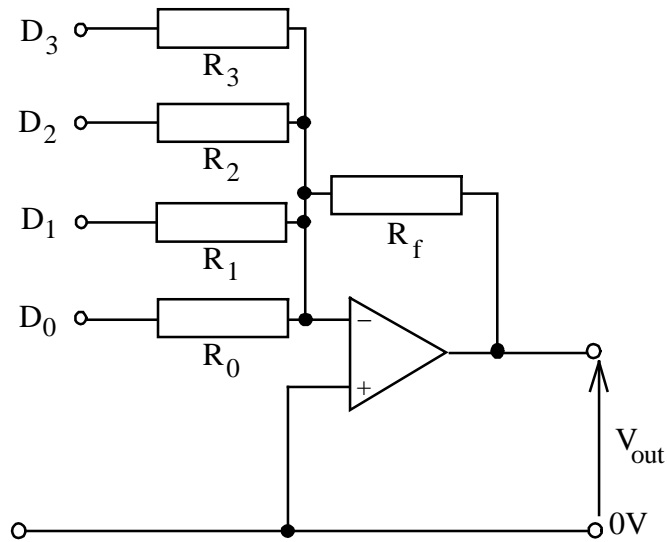
$$\text{If } R_1 = R_2 = R_3 = R \quad \text{then}$$

$$V_{out} = -\frac{R_f}{R} \left(V_1 + V_2 + V_3 \right)$$

i.e. the output voltage is proportional to the sum of the input voltages.

$$\text{If } \mathbf{V_1} = \mathbf{V_2} = \mathbf{V_3} = \mathbf{V} \quad \text{then}$$

$$\Rightarrow \mathbf{V_{out}} = -\mathbf{R_f} \times \mathbf{V} \times \left(\frac{1}{\mathbf{R_1}} + \frac{1}{\mathbf{R_2}} + \frac{1}{\mathbf{R_3}} \right)$$

i.e. the output voltage is proportional to the sum of the reciprocals of the input resistors. This circuit can be used to make a simple **Digital to Analogue Converter** (**DAC**) as is shown in the diagram below.

$$\mathbf{R_3} = \mathbf{R_f}, \qquad \mathbf{R_2} = 2\mathbf{R_f}, \qquad \mathbf{R_1} = 4\mathbf{R_f}, \qquad \mathbf{R_0} = 8\mathbf{R_f}$$

The logic inputs, $\mathbf{D_0}$, $\mathbf{D_1}$, $\mathbf{D_2}$, $\mathbf{D_3}$ all have the same voltage, with $\mathbf{D_3}$ being the most significant bit. The output voltage will therefore be directly related to the digital number applied to the inputs, but will be a negative voltage.

11.8 FILTER CIRCUITS

Capacitative reactance.

Consider the circuit diagrams below. When power is applied to circuit (a), the lamp flashes briefly but does not light. This is because there is only a brief flow of current through the lamp which charges the capacitor.

However, when power is applied to circuit (b), the lamp lights. These results suggest that a capacitor blocks direct current (dc) but allows alternating current (ac) to pass.

12V

lamp 6V, 60mA

B   A

10 μF

(a)

12V r.m.s., 50Hz

X   Y

lamp 6V, 60mA

B   A

10 μF

(b)
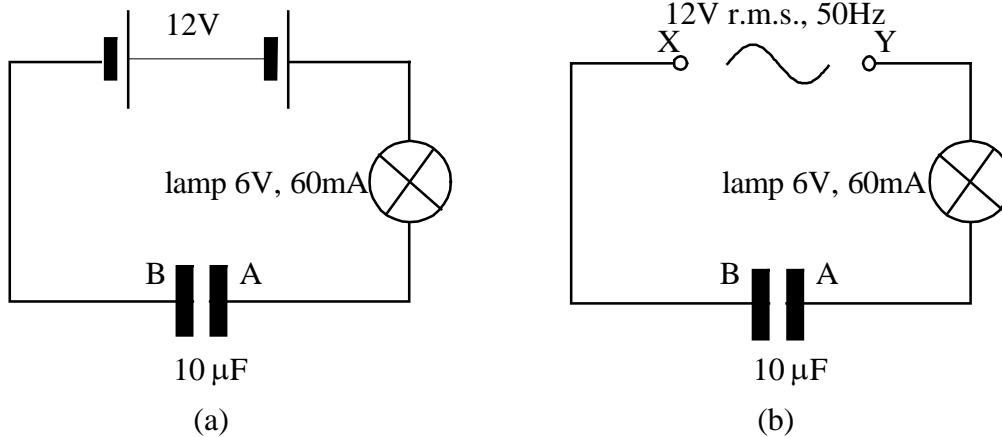
When terminal Y of the ac supply is positive, current flows and charges the capacitor with plate A positive and plate B negative. The direction of the current then reverses and the capacitor discharges. When the terminal X of the ac supply becomes positive, the capacitor charges up with the plate B positive and plate A negative, discharging again as the ac supply becomes zero at the end of the cycle. This process is repeated at the frequency of the supply. No electrons pass through the capacitor since its two plates are separated by an insulator. But electrons flow backwards and forwards in the connecting wires and this makes it appear that a current passes through the capacitor. The current flowing through the lamp can be measured using an ac ammeter.

The opposition of a capacitor to ac is called its **capacitive reactance, X_c** .

This is calculated from

$$X_c = \frac{1}{2\pi fC}$$

X_c is measured in **ohms** if **f** is in hertz and **C** is in farads.

The capacitive reactance **decreases** if either the frequency or the capacitance increases as in the diagram below.

capacitive reactance, X_C

frequency (f)

capacitive reactance, X_C

capacitance (C)
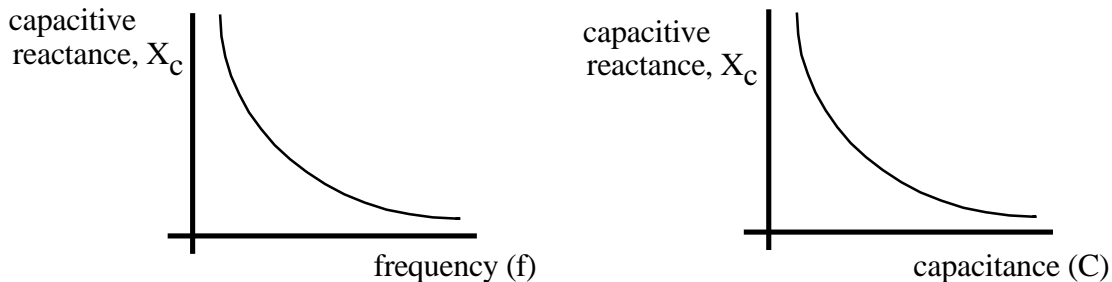
Passive RC Filters

These are used to suppress or enhance parts of a signal's frequency spectrum, e.g. to compensate for the imperfect frequency response of a transducer and so restore the frequency balance of the signal from that transducer.

Passive low pass filter.

A filter which attenuates high frequencies is known as a low pass or treble cut filter, and is shown in the diagram below. The filter allows low frequencies to pass through without much attenuation.
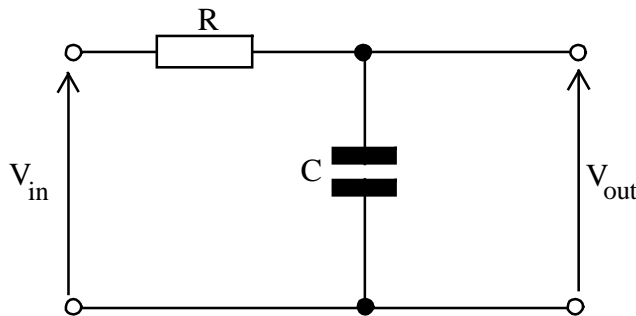
The circuit is essentially a voltage divider. To estimate the output voltage, $\mathbf{V_{out}}$, at a certain frequency, $\mathbf{f}$, first calculate the reactance, $\mathbf{X_c}$, then replace this reactance with a resistor of equal value in the voltage divider formula.

$$\Rightarrow \mathbf{V_{out}} = \mathbf{V_{in}} \times \frac{\mathbf{X_c}}{\mathbf{R + X_c}}$$

There is a phase shift of 90º between the current passing through the capacitor and the voltage across it, so the capacitor does not strictly behave like a resistor for alternating signals. The error is very small if the reactance of the capacitor is much larger or much smaller than the resistance of **R**.

Taking into account the phase shift, it can be shown that

$$\frac{\mathbf{V_{out}}}{\mathbf{V_{in}}} = \frac{1}{\sqrt{1 + \dfrac{\mathbf{R^2}}{\mathbf{X_c^2}}}} \qquad \text{(Equation A)}$$

This equation is known as the ***transfer-function*** of the filter.

The cut-off frequency, $\mathbf{f_o}$, of the filter is the frequency when the reactance of the capacitor is equal to the resistance.

$$\Rightarrow \mathbf{X_c = R} = \frac{1}{2\pi \mathbf{f_o} \mathbf{C}}$$

$$\mathbf{f_o} = \frac{1}{2\pi \mathbf{RC}}$$

Equation A can be written as

$$\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + \dfrac{f^2}{f_0^2}}}$$

So at the **cut-off frequency, f_0,**

$$\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{2}} = 0.71$$

When the frequency is below **f_0,**

$$\frac{V_{out}}{V_{in}} = 1$$

when the frequency is above **f_0,**

$$\frac{V_{out}}{V_{in}} = \frac{f_0}{f}$$

The **transfer-function** of the filter is displayed in the diagram below on a **log-log graph** of V_{out}/V_{in} against frequency. The graph can be simplified by using the
two line approximation.
For frequencies less than the cut-off frequency the graph is drawn as a horizontal line, and above the cut-off frequency the line drops at an angle of 45°.
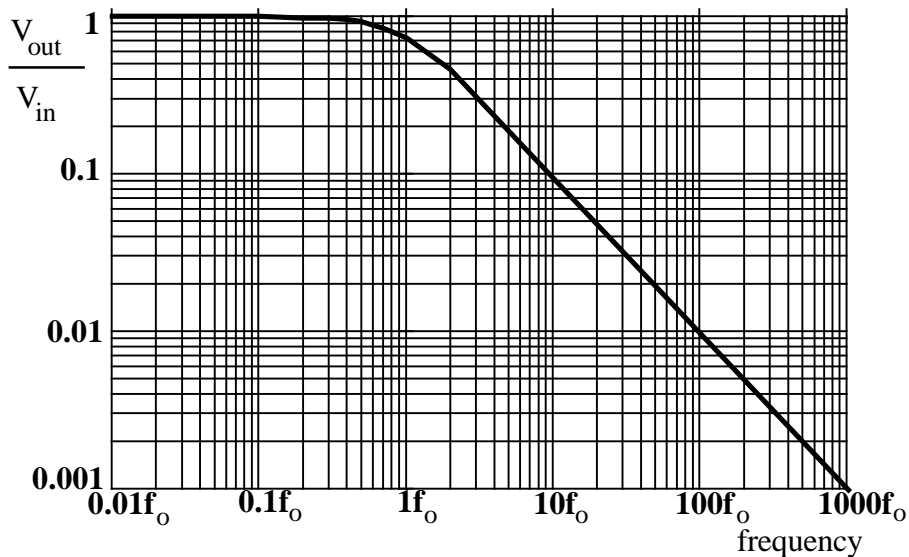
Passive high pass filter.

The circuit for a high pass or bass cut filter, allowing high frequencies to pass and suppressing low frequencies, is shown in the diagram below. The output is taken from across resistor **R**.

By a similar analysis to the passive low pass filter it can be shown that

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{R}{X_c}}{\sqrt{1 + \dfrac{R^2}{X_c^2}}} = \frac{\dfrac{f}{f_o}}{\sqrt{1 + \dfrac{f^2}{f_o^2}}}$$

Below the cut-off frequency, X_C is larger than R and so $\qquad \dfrac{V_{out}}{V_{in}} = \dfrac{f}{f_o}$

Above the cut-off frequency, X_C is smaller than R and $\qquad \dfrac{V_{out}}{V_{in}} = 1$

At the **cut-off frequency, f_o,** $\qquad \dfrac{V_{out}}{V_{in}} = \dfrac{1}{\sqrt{2}} = 0.71$
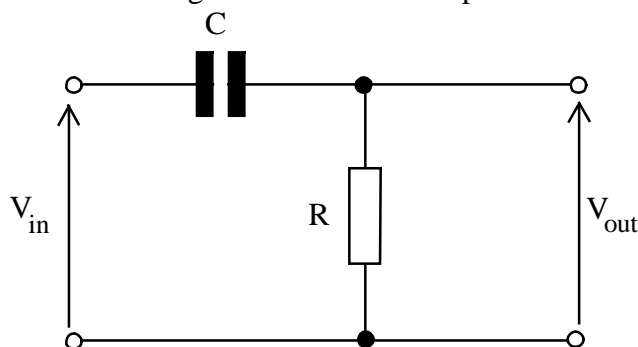
The **transfer-function** of the filter is displayed in the diagram below on a **log-log graph** of V_{out}/V_{in} against frequency. The graph can again be simplified by using the *two line approximation*.
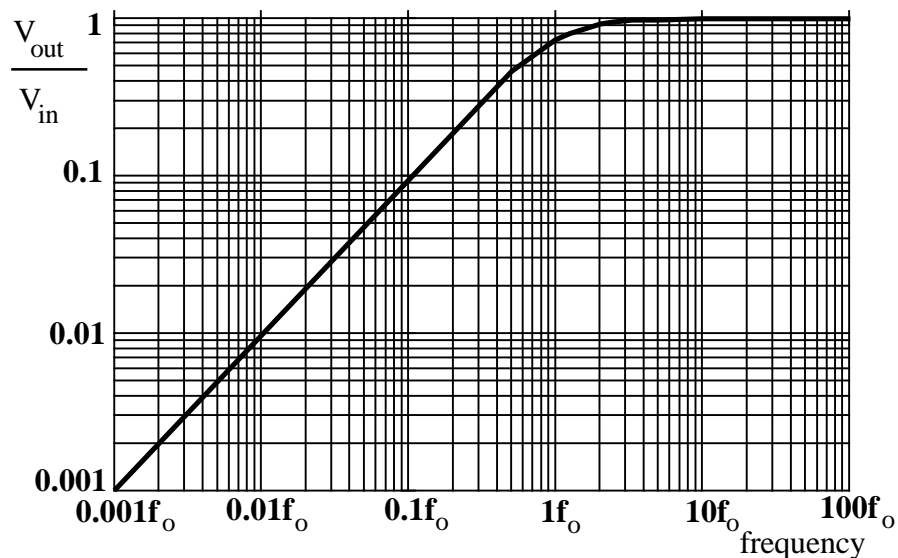
The behaviour of passive filters depends on the current supplied by them. Their performance is only as described when the output signal is fed into a very large impedance. This is easily achieved by a buffer amplifier. However the most serious disadvantage of passive filters is that they always lead to an attenuation of the signal. This can be overcome by using active filters.

Active Filter Circuits

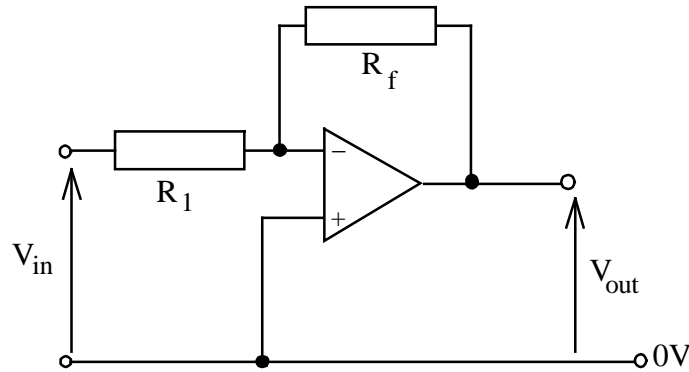Passive filters can be made into active filters by incorporating them into op-amp amplifier circuits. For convenience the inverting op-amp amplifier will be used for the following examples, but the same principles can be applied to the non-inverting amplifier as well.

An op-amp inverting amplifier is shown in the diagram below.

Its input resistance is equal to R_1. So if a capacitor is connected in series with R_1, the input circuit can be considered to be a high pass filter as shown in the diagram below.

equivalent input circuit
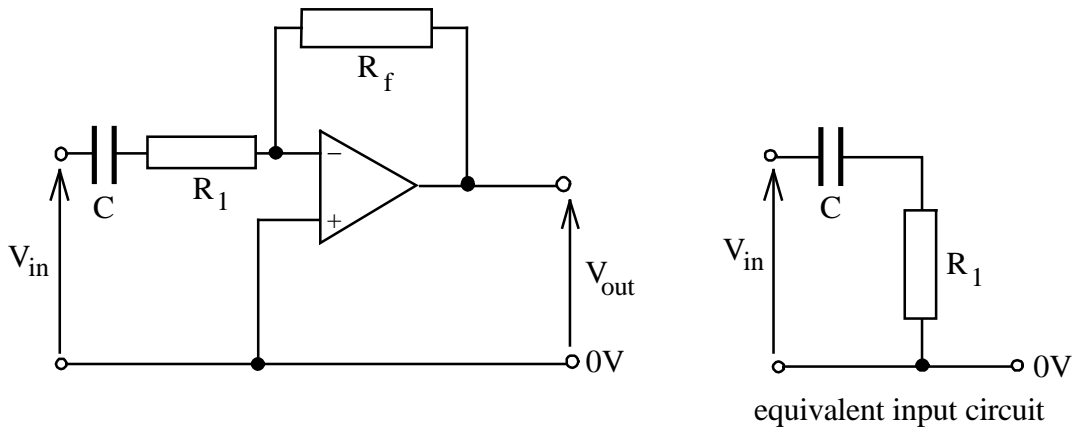
So the overall circuit will function as a high pass filter with a cut-off frequency, f_0, (i.e. the frequency at which the reactance of the capacitor equals the resistance of R_1), given approximately by

$$f_0 = \frac{1}{2\pi C R_1}$$

and a gain of

$$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1}$$

for frequencies above the cut off frequency.

If the inverting amplifier has a capacitor connected in parallel with the feedback resistor R_f, as in the diagram below, then it will function as a low pass filter.
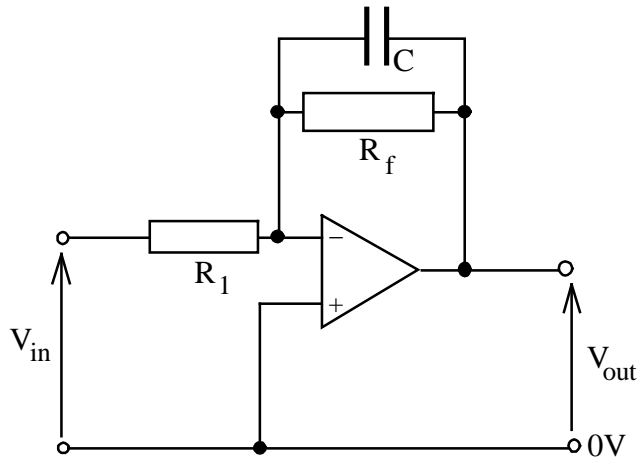
The approximate cut off frequency, f_0, (i.e. the frequency at which the reactance of the capacitor equals the resistance of R_f), is given by

$$f_0 = \frac{1}{2\pi C\, R_f}$$

and the voltage gain at frequencies below the cut-off frequency is given by

$$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_1}$$

These ideas can be combined together with an additional feedback path as in the diagram below.
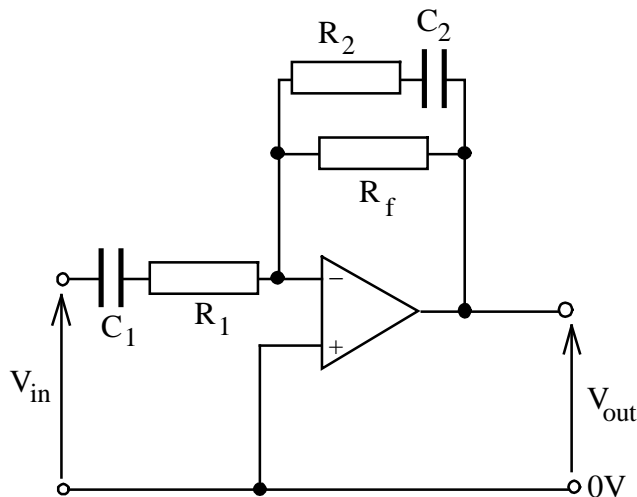
R_1 and C_1 form a high pass filter. C_2 and R_2 form a low pass filter. At low frequencies the reactance of C_2 is so large that R_2 can be ignored. At high frequencies, the reactance of C_2 is so small that R_2 and R_f are effectively in parallel, which determines the voltage gain of the system at high frequencies.

11.9 POWER AMPLIFIERS

Source Followers.

Most of the amplifiers so far examined have been voltage amplifiers. While these are fine for increasing the size of signals, they are unable to produce an output with much power. To achieve a substantial power output a circuit that provides current gain is required. Source follower circuits provide no voltage amplification but do provide considerable current amplification. The circuit diagram for a source follower is shown below.
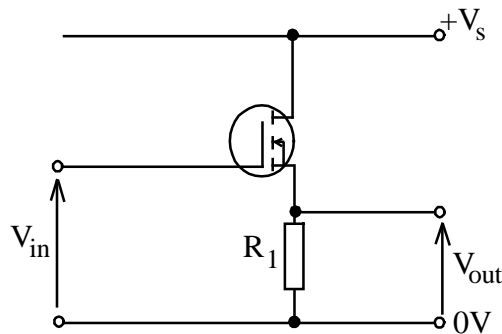

For the MOSFET circuit, as V_{in} increases so does the drain current. This causes a corresponding increase in the voltage across R_1. It can be shown that so long as the product of the mutual conductance of the MOSFET and R_1 are large, then the voltage gain of the circuit is unity. The current gain, though, is a different matter. Since the input resistance of the MOSFET is very high, there will be very little input current to the MOSFET (usually much less than 1nA). So for a drain current of 1A, the current gain will be 10^9!! This property of MOSFETs enables them to be used as very effective *Buffers*, where the output is almost completely isolated from the input.

The power gain of these circuits can be approximated by using the formula

$$\textbf{power gain} = \frac{\textbf{power output}}{\textbf{power input}}$$

The output power can be calculated from the formula

$$W = \frac{V^2}{R}$$

where V is the rms value of V_{in} and R is the load resistor R_1.

MOSFETs are voltage operated devices, unlike bipolar transistors which are current operated. To make a drain current flow a voltage is applied between the gate and source. The relationship between this gate voltage and the drain current is known as the **Mutual transconductance** (**g**), where

$$g = \frac{\Delta I_d}{\Delta V_{gs}}$$

The unit of **g** is siemens (S) if **I** is in amps and **V** is in volts.
Value of **g** ranges from 20mS to 30S or more for high power devices.

For the source follower the input resistance is so large that the input power is almost negligible. This leads to a power gain that is very large.

Push-Pull Output Circuits.

A single transistor or MOSFET amplifier, when suitably biased, is known as a CLASS A amplifier and is not very efficient in terms of power supplied compared to the useful power delivered to the load. The theoretical maximum efficiency can only be 50% and in most cases an efficiency of between 10% and 20% can be expected. While this is of little importance for small signal amplifiers it becomes a serious problem when a power output of 100W or more is required for an audio amplifier! It is an interesting exercise to calculate the power dissipated in the transistor or MOSFET in this case.

The main reason for this gross inefficiency is the need to bias the drain to be at a voltage that is half of the supply voltage. A way of overcoming this difficulty is to use two power supplies, one positive and the other negative and then use two matched output MOSFETs, one n-channel and the other p-channel, connected as source followers, to provide the power gain. It is important that both MOSFETs are matched so that they have very similar characteristics. A very basic MOSFET push-pull amplifier circuit is shown in the diagram below.
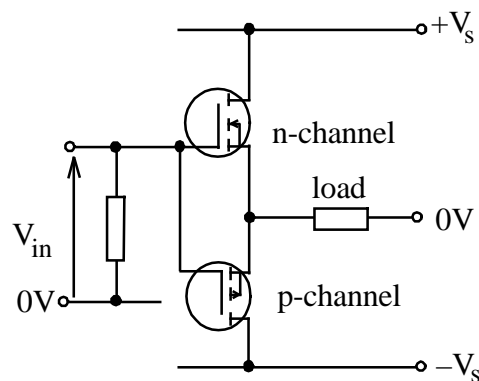
In this circuit, no steady current flows through the MOSFETs. Consider an input signal applied to the circuit. Because of the non-linearity at very small values of the gate to source voltage V_{gs}, the output will be distorted as shown in the oscilloscope diagram on the next page.

The distortion that occurs in the output is called **CROSS-OVER DISTORTION**, and is due to the non-linearity of the MOSFETs for small input voltages. Such distortion may be acceptable at very large output power levels, but at low output power levels it would be unacceptable.

Since current only flows through the MOSFETs when there is an input signal greater than approximately 0.5V, the efficiency of the circuit (**power-out / power-in**) is high and can approach 90%.
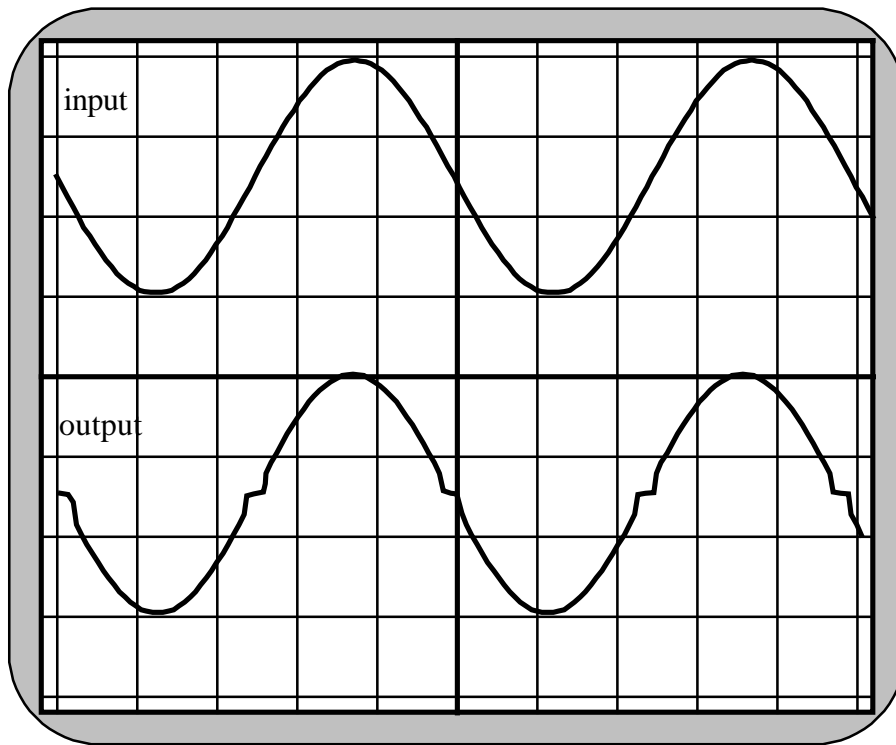
To eliminate the cross-over distortion it is necessary to ensure that the MOSFETs are biased so that a small current (*quiescent current*) flows through them even when there is no input signal. This reduces the effect of this type of distortion by overcoming the non-linearity of the MOSFETs. The overall efficiency of the circuit is reduced to about 70% , but this is dependent on the quiescent current flowing through the MOSFETs.

There are many ways of providing bias for the MOSFETs, one such arrangement is shown in the diagram below.
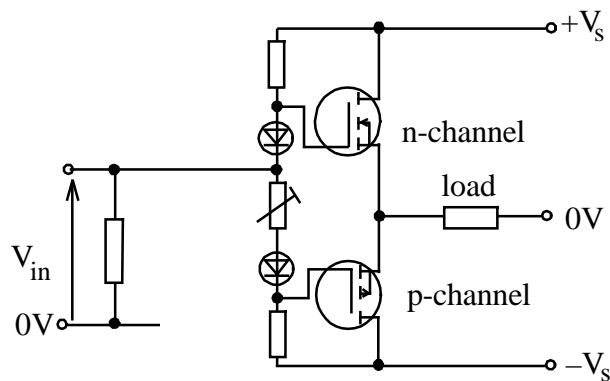
The variable resistor enables the quiescent current to be set for the required value. This will range from a few mA for a low power amplifier up to 100mA or more for a high power amplifier. The use of diodes provides some degree of temperature stability, for as the temperature of the diodes rise, the voltage across them falls and so reduces the voltage applied to the MOSFETs. MOSFETs are also inherently more temperature stable than transistors. As the temperature of a MOSFET increases, its channel resistance increases and so reduces the current flowing through it, so reducing its temperature.

Assuming that the power supply for a push-pull amplifier is symmetrical ($\pm\,\mathbf{V_s}$) then the maximum power output from the amplifier can be estimated as follows.
Assume that when fully conducting, there is 2V between the drain and source of the output MOSFETs.
Therefore the amplitude of the voltage that can appear across the load is

$$\mathbf{(V_S - 2)\ volts}$$

For a sine wave, this results in a maximum rms output voltage of

$$\frac{\mathbf{(V_s - 2)}}{\mathbf{1.414}}\ \mathbf{volts}$$

The power is now calculated from

$$\mathbf{P = \frac{V^2}{R}}$$

$$\Rightarrow \mathbf{P = \frac{\left\{ (V_s - 2) \big/ 1.414 \right\}^2}{R}}$$

$$\Rightarrow \mathbf{P = \frac{(V_s - 2)^2}{2R}}$$

where $\mathbf{V_s}$ is the supply voltage of one of the supplies and $\mathbf{R}$ is the load resistance.

e.g. If an amplifier has a power supply of $\pm$ 50V and an 8Ω speaker connected to it then the maximum output power is

$$\mathbf{P = \frac{(50 - 2)^2}{2 \times 8} = \frac{48^2}{16} = 144W}$$

$$\mathbf{P = 144W}$$

If the amplifier is 75% efficient then the output transistors will be dissipating 48W, which will result in the need for some way of removing all of the excess heat that this creates.

Experimental Push-pull amplifier.

A simple but effective push-pull amplifier circuit is shown below. It can be cheaply, quickly and easily constructed on a protoboard and modified to demonstrate the effects of cross-over distortion and clipping. The circuit uses a TL071 op-amp, a n-channel MOSFET type IRF630 and a p-channel MOSFET type IRF9630. Both MOSFETs need a gate to source voltage of approximately 3V before they begin to allow current to pass from drain to source. To help provide this bias voltage, red LEDs are used since they need approximately 2V across them before they conduct.

The circuit below contains no biasing of the output MOSFETs and negative feedback is restricted just to the op-amp. The output contains significant cross over distortion which can

be observed on an oscilloscope and heard in the loudspeaker. The 0V from the power supply should be connected directly to the 0V point on the speaker. A wire should then link this point to the 0V of the input. This will help to keep the circuit stable.
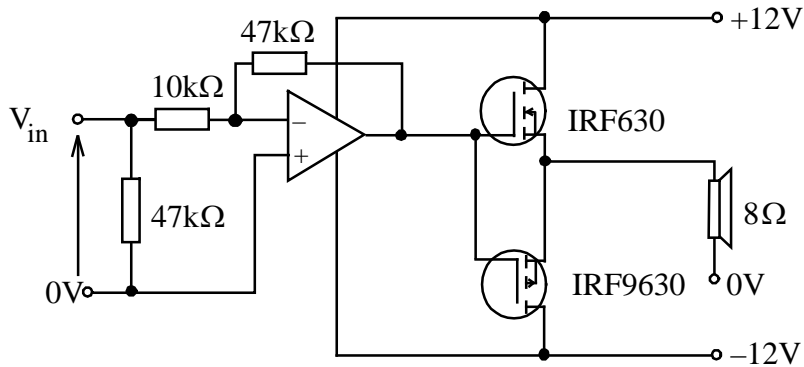
The next improvement is to provide some bias for the MOSFETs as shown in the diagram below. The two LEDs are the standard red type and the two diodes are 1N4001 types.
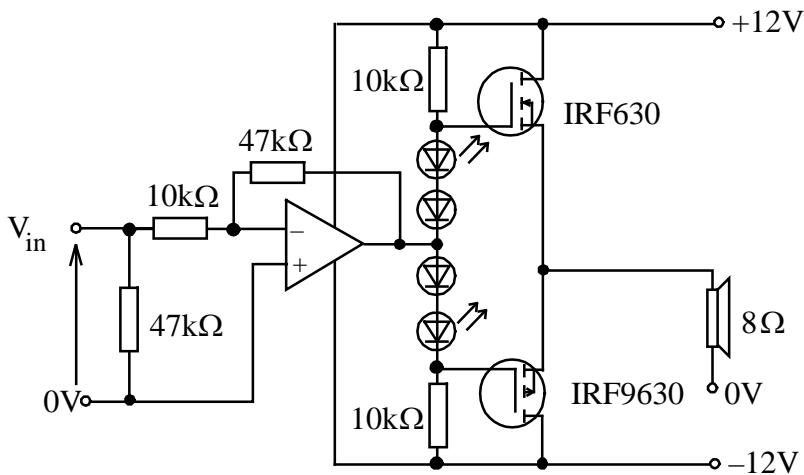
The final improvement is to incorporate the MOSFET output stage into the negative feedback loop as shown below.
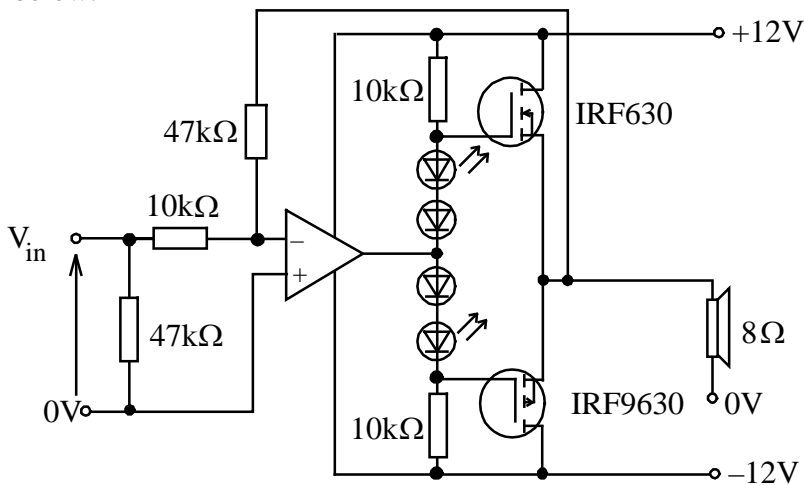
The metal tab of each MOSFET is connected to its drain so each MOSFET should be mounted on its own heatsink.

Heat Sinks

Whenever large currents are being controlled by semiconductors there is inevitably heat dissipated within the semiconductor device. The maximum temperature that a semiconductor can withstand is about 120^OC before it becomes damaged. To keep the temperature within safe limits, the semiconductors must be physically secured to materials that will conduct the heat away from them and allow the heat to dissipate. Such materials are usually metals and they are available in a variety of shapes and sizes.

There are four main ways in which the semiconductor can be kept cool,

a)   by physically attaching the semiconductor to a metal heat sink, (usually made from aluminium); to conduct away the heat,

b)   by allowing the semiconductor to cause convection currents by providing a large surface area of heat sink and by ensuring that there is a good, unrestricted   flow of surrounding air,

c)   by painting the heat sink matt black and by having a large surface area to allow the heat to be radiated away,

d).   by using a fan to blow cooler air over the semiconductor.

The large surface area of a heat sink is achieved by having fins, which when arranged vertically will ensure that the surrounding air is warmed and is then able to move away allowing cool air to replace the warm air. This cooling can be further enhanced by using a fan to blow cool air through the fins of the heat sink.

A problem that occurs with cooling semiconductors is that the metal cases of the semiconductors are not usually electrically isolated. This means that they cannot simply be bolted onto a metal heat sink since their cases would short circuit together. This problem can be overcome by using a thin mica or mylar washer as an electrical insulator in-between the semiconductor and the heat sink. To ensure a good thermal contact between the semiconductor and the heat sink silicone grease is often smeared on each side of the insulator.

Heat sinks are usually rated in terms of their temperature increase per watt of power dissipated. This quantity is known as **Thermal Resistance** and is measured in degrees C per watt (^{O}C/W). A small heat sink fitted to a small transistor may have a thermal resistance of 30^OC / W, which means that for every watt of power dissipated in the transistor, the case temperature can be expected to **rise** by 30^OC.

When deciding what the thermal resistance of a heat sink needs to be, there are several assumptions to make. These are:-

a).   the maximum permitted temperature of the semiconductor case, which should be no more than 100^OC,

b).   the maximum ambient air temperature, which should be taken as 35^OC to allow for use in warmer countries,

c).   the maximum power that the semiconductor is ever going to dissipate even under fault conditions,

d).   the thermal resistance between the semiconductor and the air is very large but the thermal resistance between the semiconductor and the heat sink is very small and can be ignored. If silicone grease is used then this is a reasonable approximation.

e.g.   If the maximum current passing through a MOSFET is 5A when there is a drain to source voltage of 6V, calculate the thermal resistance of the heat sink required.

The maximum power dissipation in the transistor $= \textbf{V} \times \textbf{I} = \textbf{6} \times \textbf{5} = \textbf{30W}$,

The maximum temperature rise allowed is from 35°C to 100°C, a rise of 65°C.

$$\Rightarrow \textbf{thermal resistance} \ = \frac{\textbf{temperature rise}}{\textbf{power dissipated}}$$

$$\textbf{thermal resistance} = \ \frac{\textbf{65}}{\textbf{30}} = \textbf{2.17}^{\textbf{o}} \textbf{C} / \textbf{W}$$

This would be a fairly substantial heat sink and in practice a 2°C / W heat sink would be selected from one of the many electronics catalogues that are available.
Although the assumptions made do produce errors, all the errors err on the side of caution and so the only real effect of the errors is that the heat sink may be a little larger than absolutely necessary.

Thermal Runaway

Both transistors and MOSFETs have their advantages and disadvantages as high power output devices. Some have already been mentioned in earlier sections.
Bipolar transistors are current operated devices which means that they have a low input resistance. Their current gain is not constant. It varies with collector current, decreasing as collector current increases. It also varies with temperature, increasing substantially as temperature increases. They have a small voltage across the collector -emitter junction when they are saturated (usually about 0.2V), which ensures that they dissipate little power when saturated. Transistors also suffer from a problem known as *Second Order Current Breakdown*. This occurs when there is high collector currents and a large voltage between the collector and emitter. The collector current, instead of passing uniformly through the collector-base-emitter junction, become channelled through a small section causing local heating which destroys that section of the junction. The destruction of the remaining part of the junction quickly follows.
As a result of the current gain being a function of both temperature and collector current, temperature being the dominant effect, a phenomenon known as thermal runaway can occur with bipolar transistors. When the transistor is passing a large current, it dissipates power and warms up. This causes the current gain to increase, thereby causing a larger collector current to pass. This in turn leads to a larger dissipation of power, and a corresponding increase in temperature. This in turn leads to an increase in current gain etc. The result, especially for a circuit with no negative feedback to control temperature, is rapid over dissipation of power and the corresponding destruction of the transistor. It is important that this effect is taken into account when designing high power circuits.

MOSFETs are voltage operated devices and so have a very large input resistance (though not necessarily a high input impedance, especially at high frequencies). The mutual conductance, once the drain current is above a few mA, is fairly constant, and is not significantly affected by either temperature or drain current. Their drain to source resistance (the resistance of the conducting channel) is now low for modern MOSFETS, being typically 0.5Ω for medium power audio amplifier devices. This means that they dissipate more power than a bipolar transistor. They do not however, suffer from either second order breakdown or thermal runaway. In fact they are inherently temperature stable, for as the temperature increases, the

channel resistance between drain and source increases, which leads to a reduction in drain current and, correspondingly, a reduction in temperature.

Any circuit designer using power MOSFETs should be aware of their extremely good high frequency response. A common problem encountered when building high power audio amplifiers with MOSFET output devices is that the amplifier will be unstable and may produce many watts of very high frequency oscillations (>10MHz) to the speakers. This has the effect of causing excessive power dissipation of the output MOSFETs as well as the speakers. It also does little for the quality of the sounds being amplified!

APPENDIX A

Using Multimeters

Analogue Multimeter

An analogue multimeter consists of a sensitive moving coil meter (often 50μA full scale deflection, FSD). The deflection of the pointer over a scale represents the value of the quantity being measured, figure A.1.

To allow the meter to measure larger currents, low value resistors are connected in parallel with the meter by the range switch. To allow the meter to measure voltages, high value resistors are connected in series with the meter again by the range switch. As a result of the current that passes through the meter when it is measuring voltages, the meter affects the circuit being tested and so can alter the quantity to be measured.

A voltmeter should have a very large resistance so that only a very small current passes. The sensitivity of a voltmeter is expressed in ohms per volt, i.e. the resistance that the meter must have when reading 1 V full scale deflection. So a 50 μA meter will need to have a total resistance of 20 kΩ when it has a FSD of 1V. The sensitivity of such a meter is then 20,000 Ω/V.

On the 10 V range its resistance is therefore 200 kΩ, the increase in resistance being due to extra resistors connected in series by the range switch. For a given sensitivity the higher the voltage range the less the disturbance to the circuit.
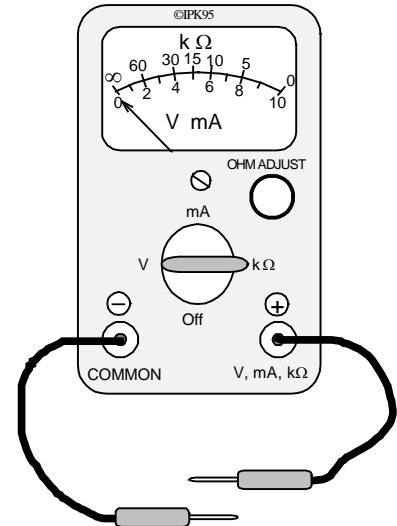

Figure A1

Digital multimeter

The reading on the decimal display is produced by a voltage measuring analogue to digital converter. The binary output from the A to D converter is applied to a decoder which controls the display, figure A.2. Very small input voltages (a few millivolts) are amplified before being measured. For varying voltages a latch system is used to hold the display steady at the latest value while a further sampling occurs. With extra internal circuitry brought in by various range switches, currents and resistances can be measured.

The advantages of the digital over the analogue multimeter include:-

The input resistance on voltage ranges is high (11MΩ) and is the same on all ranges so the disturbance effect on the circuit under test is reduced.

Errors are less likely to occur from reading the wrong scale or from estimating the reading when the pointer is not exactly over a marking on the scale.

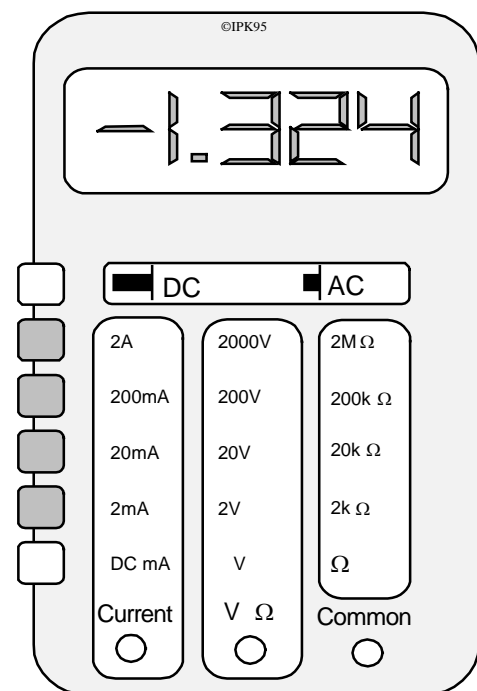It has a much higher operating frequency on its ac ranges.

Figure A.2

APPENDIX B

Using An Oscilloscope

The oscilloscope is a very useful test instrument in electronics. It is essentially a voltmeter with a very rapid response to changing input voltages. A diagram of a typical modern oscilloscope is shown in figure B.1.
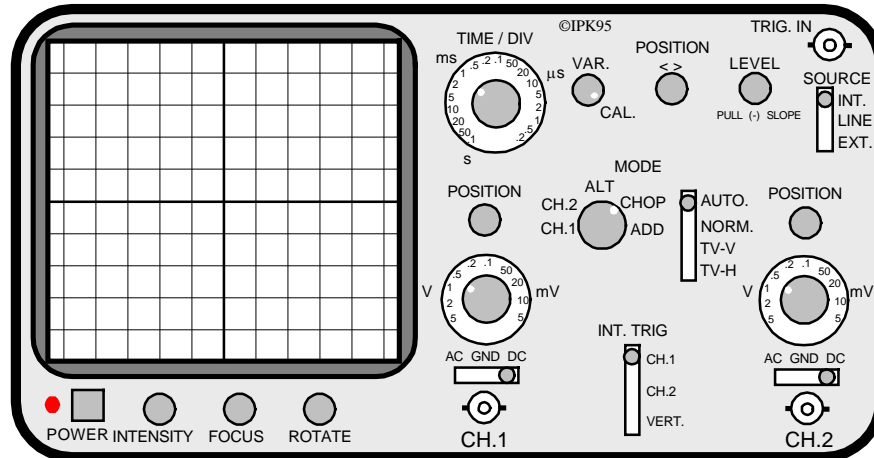

Figure B.1

An oscilloscope can be used for measuring the following quantities:-

the peak voltage of a signal,
the peak current of a signal by measuring the peak voltage across a known resistor,
the time period of a signal, from which the frequency can be calculated,
the phase difference between two signals, using a dual trace oscilloscope.

Measurement Of Peak Voltage And Frequency

a)   Set up the oscilloscope according to the manufacturer's instructions.
b)   Connect the voltage signal to the input terminals.
c)   Adjust the y gain control so the trace covers at least half the height of the screen.
d)   Adjust the trigger control so that the trace is stable.
e)   Adjust the time base control to give between three and six cycles.
f)   Measure the vertical peak to peak displacement of the signal on the screen in cm and divide by two to find the amplitude. Use the **y gain sensitivity** setting in V/cm to calculate the amplitude.

Peak voltage (V) = amplitude (cm) x y gain sensitivity (V/cm)

g)   Measure the horizontal distance occupied by one cycle on the screen and use the time base setting to calculate the time period.

Time period, T(ms) = distance of one cycle in cm x time base (ms/cm)

To calculate the frequency use $f = \dfrac{1}{T}$

eg. Consider figure B.2.

Y sensitivity = 2V/cm.
Time base setting = 5ms/cm

From figure B.2,
peak to peak value is 4cm.
So the amplitude of the signal
= 2.0cm.
Voltage amplitude = 2cm x 2V/cm
                          = **4.0V**

From figure 1.32 the period distance of the
signal = 4.0 cm
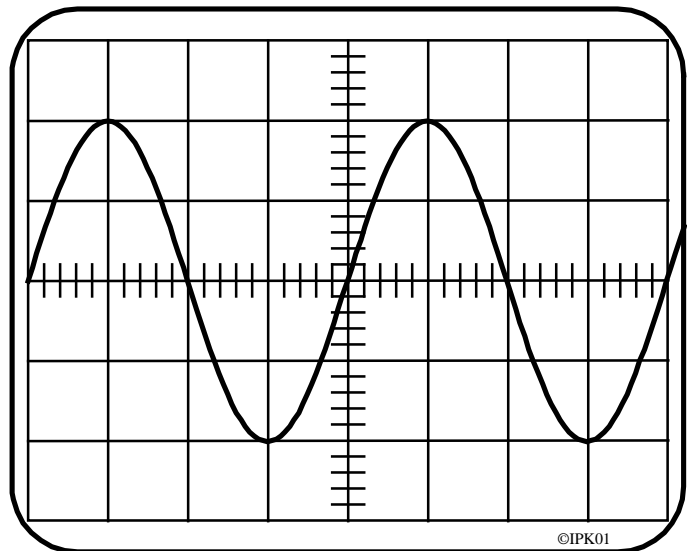Time period, T = 4.0cm x 5ms/cm
                          = **20ms**

Frequency $f = \dfrac{1}{T} = \dfrac{1}{20ms} = $ **50Hz**

Figure B.2

Measurement Of Phase Difference Between Two Signals

Use a dual trace oscilloscope to obtain the two signal traces.
Measure the horizontal distance, in cm, between corresponding peaks of the two signals and
the period distance of one of the waves.
Determine the phase difference using the fact that one period distance represents 360º.

eg.   Calculate the frequency and phase
difference for the signals in figure B.3, if
the time base is set to 0.2ms/cm.

Period distance of each wave
                          = **4.8cm.**

Time period, T = 4.8cm x 0.5ms/cm
                          = **0.24ms**

Frequency
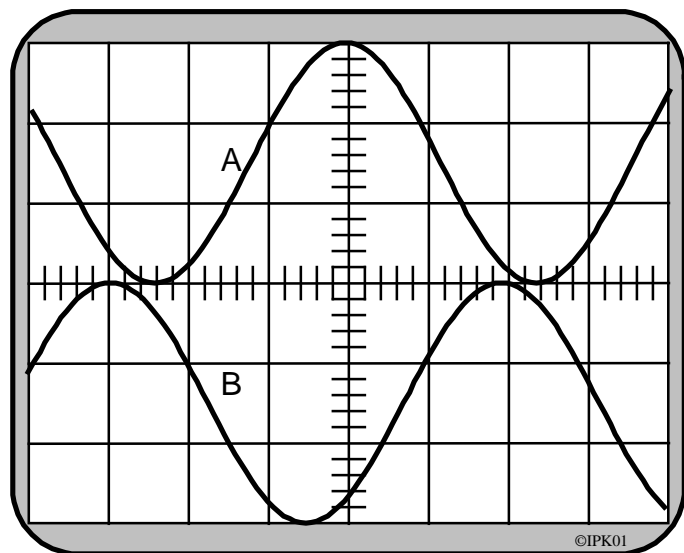$f = \dfrac{1}{T} = \dfrac{1}{0.24\,ms} = $ **4.17kHz**

Figure B.3

Phase difference = 2.0cm. But 360 º represents 4.8 cm.
So 1.0 cm represents 75º. Therefore the phase shift is 2 x 75º = 150º.

Signal A leads signal B by 150º.

APPENDIX C

Types And Uses Of Capacitors

| Types	Polyester	Mica	Poly-propylene	Ceramic	Electrolytic	Metallised film	Poly-carbonate	Poly-styrene	Tantalum
Range	10nF – 10μF	1pF – 10nF	1nF – 1μF	1pF – 470nF	100nF –1F.	100nF – 16μF	10nF – 10μF	1pF – 10nF	10nF – 100μF
Tolerance	±20%	±1%	±20%	±20%	±50%	±20%	±20%	±2.5%	±20%
Stability	Good	Excellent	Good	Fair	Poor	Fair	Excellent	Good	Fair
Working voltage	Up to 400V	Up to 400V	Up to 1500V	Up to 1000V	Up to 1000V	Up to 600V	Up to 600V	160V	Up to 63V
Leakage current	Low	Low	Low	Low	High	Small	Low	Low	Small
Temperature coefficient	+200 ppm per ^{O}C.	+50 ppm per ^{O}C.	-200 ppm per ^{O}C.	-5000 to +100 ppm per ^{O}C.	>1000 ppm per ^{O}C.	+200 ppm per ^{O}C.	+60 ppm per ^{O}C.	-50 to +100 ppm per ^{O}C.	+200 ppm per ^{O}C.
Uses	General.	Tuned circuits, Filters, Oscillators.	High alternating voltage circuits.	Decoupling, temperature compensation in oscillators.	Decoupling, smoothing in power supplies.	High voltage power supply smoothing.	Filters, oscillators and timers.	Filters, oscillators.	General, timing, decoupling.

APPENDIX D
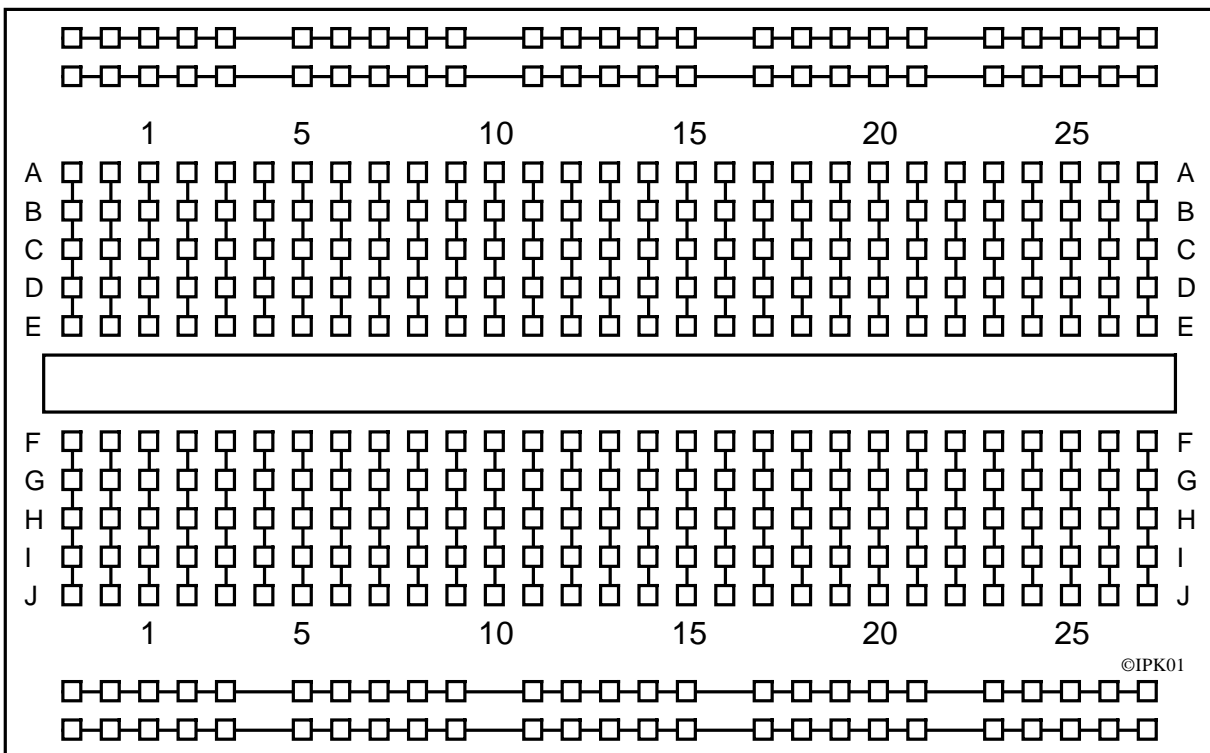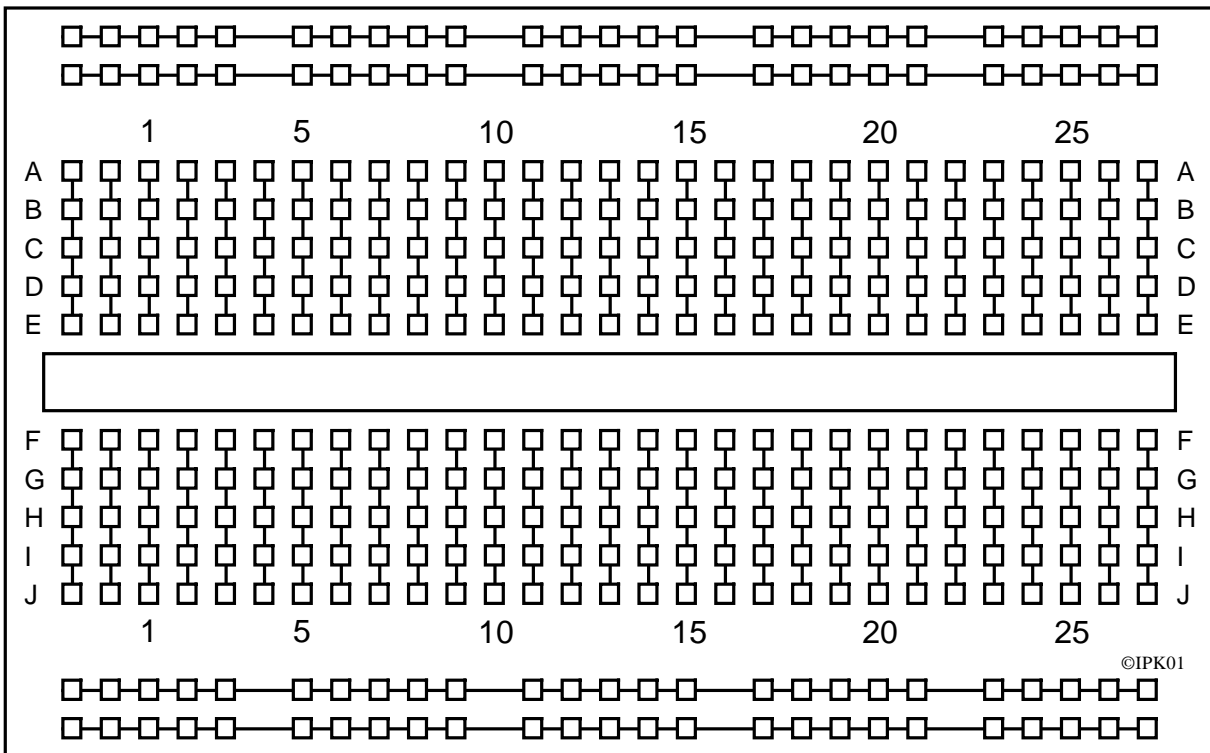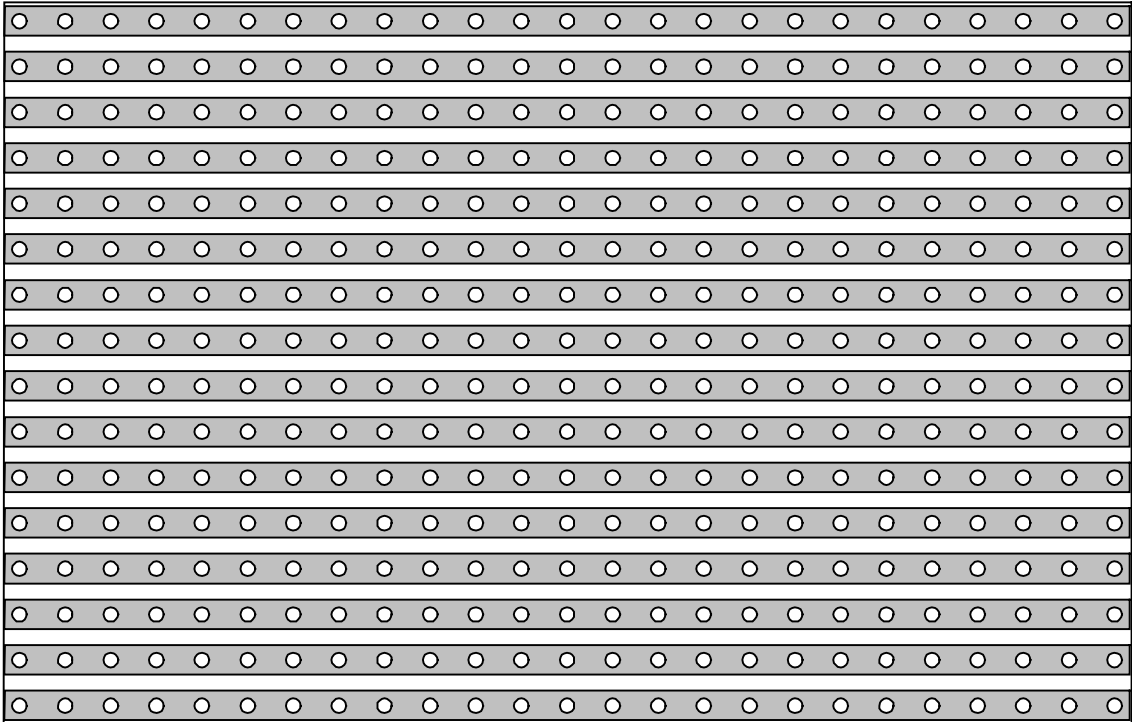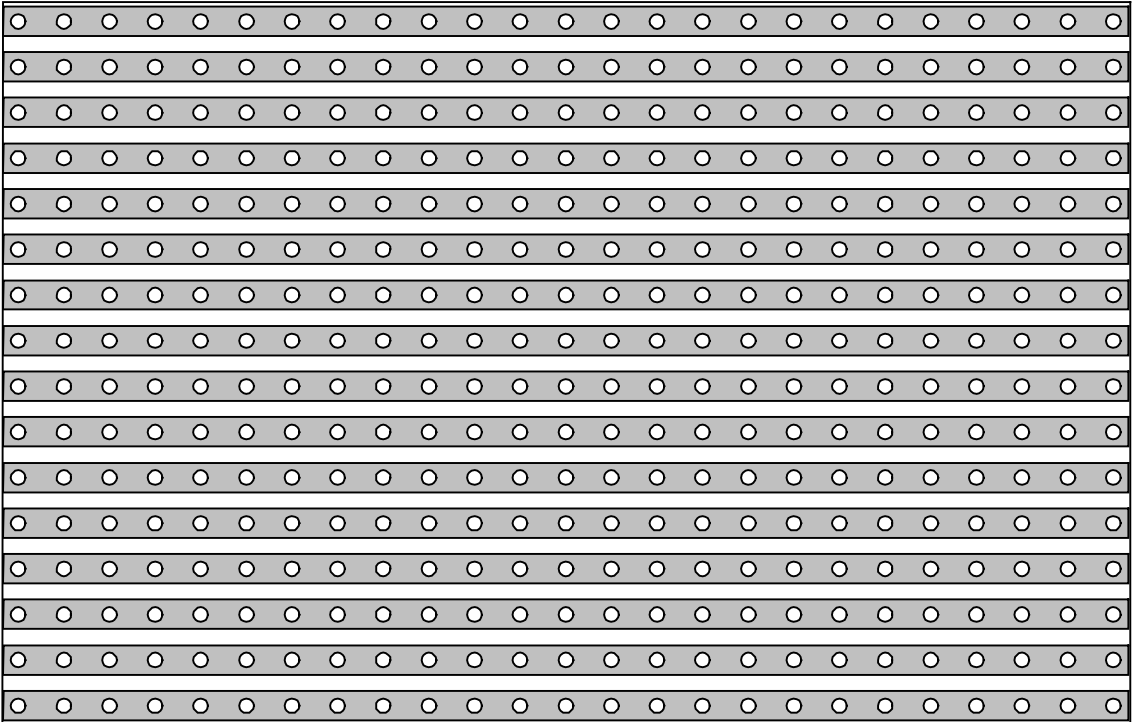
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APPENDIX E

APPENDIX F

Here is some of the AS electronics specification (exam syllabus) in a slightly modified form. You should use the specification to maximise your marks when preparing for exams or completing coursework. For the latest full specification see http://www.aqa.org.uk/ .

AS Module 1 (ELE1)
Foundation Electronics
90 marks (30% of AS marks)

Candidates should be able to:

10.1 System synthesis

recognise that simple systems consist of an input, a process, an output and possibly feedback;
analyse and design system diagrams;
represent complex systems in terms of sub-systems;
describe one modern electronic system which makes use of several sensors.

10.2 Logic gates and Boolean algebra
Introduction

identify and use NOT, AND, OR, NAND, NOR and EX-OR gates in circuits;
construct and recognise truth tables for these gates and simple combinations of gates with up to four inputs to the system;
use combinations of these gates to form other logic functions;

Boolean algebra

generate the Boolean expression from a truth table or logic diagram.

10.3 Current (I), voltage (V), power (P), resistance (R)

understand the need for identifying a zero volt point in a circuit;
define power as $V I$;
define resistance as $\dfrac{V}{I}$;
calculate the combined resistance of resistors connected in series and/or parallel;
select appropriate preferred values from the E24 series;
identify resistors using the colour code and BS 1852 code.

10.4 Diodes
Light emitting diodes

sketch and interpret I . V characteristic curves of LEDs and
calculate the value of the series resistor for dc circuits;

Silicon diodes and zener diodes

sketch I . V characteristics for silicon diodes and zener diodes;
select appropriate silicon diodes and zener diodes from given data sheets;
describe how a zener diode can be used with a current limiting resistor to form a simple regulated voltage supply;
calculate the value of a suitable current limiting resistor.

10.5 Resistive input transducers
interpret and use characteristic curves;

Light dependent resistors, thermistors and variable resistors
describe the use of LDRs and negative temperature coefficient thermistors in a voltage dividing chain to provide analogue signals;

Voltage dividers
calculate suitable values for series resistors for use with and for protection of LDRs and thermistors;
perform calculations on voltage dividers consisting of resistors and devices described above.

10.6 Transistors and MOSFETs
npn junction transistor
describe its use as a switch;

n-channel (enhancement mode) MOSFETs
describe its use as a switch;
compare the advantages and disadvantages of a MOSFET with a junction transistor when both are used as switch.

10.7 Output devices
Electromagnetic relays, solenoids, buzzers and motors
describe their use, but not construction details;
understand and explain circuit protection provided by a diode in parallel with a relay;
understand and use NO and NC notation.

10.8 Operational amplifiers
General properties
know the characteristics of an ideal op-amp and be aware that the characteristics of a typical op-amp may be different;
know the difference between inverting and non-inverting inputs;
understand power supply requirements and output voltage swing limitations of real op-amps leading to saturation;

The op-amp as a voltage comparator
understand and explain the use of an op-amp in a comparator circuit.

10.9 Capacitors
understand that a capacitor, whether isolated or as part of a circuit, is capable of storing electrical charge and energy;
realise that the farad is a large unit and that practical capacitors are usually measured in pF, nF or μF;
calculate the combined capacitance of capacitors connected in seriesand/or parallel;
select appropriate capacitors given data on maximum working voltage, temperature coefficient, polarisation and leakage current.

10.10 RC networks (dc only)

understand the meaning of and calculate the value of the time constant for RC circuits;
know that after one time constant:

$V = 0.63V_s$ for a charging capacitor,

$V = 0.37V_s$ for a discharging capacitor, where V_s is the supply voltage and V is the voltage across the capacitor;

know that:

$V = 0.5V_s$ after time $0.69RC$,

$V \sim V_s$ after time $5RC$ for a charging capacitor,

$V \sim 0$ after $5RC$ for a discharging capacitor;

sketch voltage/time graphs for charging and discharging.

10.11 555 timer circuit
555 monostable circuit

draw, recognise and use the circuit diagram for a 555 monostable, treating it as a functional block;
calculate its time period using $T = 1.1\ RC$;

555 astable circuit

draw, recognise and use the circuit diagram for a 555 astable, treating it as a functional block;

calculate frequency using $f = \dfrac{1.44}{(R_A + 2R_B)\,C}$;

calculate the time that the output is low (t_L) using
$t_L = 0.7\ R_B C$;

calculate the time that the output is high (t_H) using
$t_H = 0.7\ (R_A + R_B)C$.

AS Module 2 (ELE2)
Further Electronics
120 marks (40% of AS marks)

Candidates should be able to:

11.1 Design and simplification of combinational logic systems
design a logic system from a truth table or description using combinations of gates;
simplify logic systems using either Boolean algebra or Karnaugh maps;
convert logic systems comprising mixed gates into NOR or NAND gates only;
explain the operation of combinational logic systems.

11.2 Sequential logic systems
draw a bistable latch based on NAND gates and describe its function;
draw the symbol for a D-type flip-flop and describe its function;
describe the use of D-type flip-flops to make a shift register;
explain the operation of monostable circuits based on NAND gates and estimate the time period using $T \sim RC$;
explain the operation of an astable circuit based on NAND gates andestimate the operating frequency using $f \approx \dfrac{1}{2RC}$

11.3 Counters
describe the use of feedback to make a D-type flip-flop divide by 2;
convert a 4-bit binary number to decimal or HEX notation;
design 4-bit up or down counters based on rising edge triggered D-type flip-flops;
design 4-bit modulo-N counters and draw timing diagrams for these counters;
describe the use of a BCD or HEX decoder with a seven-segment display.

11.4 Operational Amplifiers
define the bandwidth of an amplifier as the frequency range over which the voltage gain is within 70% of maximum;
know that for a real op-amp system the product *gain × bandwidth* isconstant;
use the equation $voltage\ gain = \dfrac{V_{out}}{V_{in}}$

11.5 Inverting amplifier
draw and recognise the inverting amplifier circuit and describe its applications;
use the formula $\dfrac{V_{out}}{V_{in}} = -\dfrac{R_f}{R_i}$

know that the input resistance is equal to the value of the input resistor.

11.6 Non-inverting amplifier

draw and recognise the non-inverting amplifier circuit;

use the formula $voltage\ gain = 1 + \dfrac{R_f}{R_i}$

know that the input resistance is equal to that of the op-amp;
draw and recognise a voltage follower (buffer) based on a non-inverting op-amp;
show that the voltage follower has a gain of 1;
describe and explain a use for the voltage follower;
describe the effects of negative and positive feedback in op-amp circuits.

11.7 Summing amplifier

draw and recognise a summing amplifier circuit;
describe and explain applications, including mixing audio signals and digital to analogue conversion;
calculate resistor values for the above applications;
use the formula

$$V_{out} = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

11.8 Filter circuits

calculate the reactance of a capacitor using the formula

$$X_C = \frac{1}{2\pi R C}$$

draw and explain passive filters using RC circuits;
draw and explain first order active filters including treble cut, treble boost, bass cut and bass boost;
calculate the break point of active filter circuits.

11.9 Power amplifiers

describe and recognise a source follower as a power amplifier;
draw circuits for push-pull output circuits using p- and n- channel enhancement mode MOSFETs;
explain the operation of push-pull output circuits;
explain crossover distortion and describe how it can be reduced;
describe the advantages of push-pull output circuits over single ended output circuits;
estimate the maximum power output from a push-pull circuit;
calculate the power dissipated in a transistor and select an appropriate heat sink;
explain the features of heat sinks which make them efficient.

AS Coursework (ELE3)
Electronics Project
90 marks (30% of AS marks)

The coursework undertaken by the candidates will be to design and construct a single artefact to satisfy an initial design problem identified by the candidate. The work for the coursework unit is expected to be an independent piece of work carried out alongside the theoretical studies of the candidates. The aim for the candidate is to design, assemble and evaluate an electronic artefact and produce a written report of the work.

Candidates should be encouraged to select projects in which they are interested and which are considered achievable. Teachers should also ensure that the work undertaken is both of an appropriate standard and within the capability of the candidate. Having decided upon the aim of the project the candidates should undertake appropriate research so that a list of performance parameters (Specification) can be given. It is expected that the specification will contain realistic numerical values against which the final performance of the work can be judged. Candidates are expected to consider alternatives and give reasons for selecting the chosen solution.

The overall system for each module should be developed as subsystems which should be tested and evaluated in isolation before being incorporated into the complete system. This will ensure that the complete system grows by a gradual and incremental process, having been assessed at each stage of its development.

Candidates will be expected to develop their coursework systems on protoboard and may use computer simulations to help them. The systems can be left in protoboard form; there is no requirement for candidates to transfer their work to strip board or printed circuit board. For all modes of circuit, the layout and mounting of components, section and wiring should be neat and logical in order to assist in the design, testing and fault finding processes. Candidates will be expected to undertake Risk Assessments during their coursework in order to ensure the safety of themselves, associated workers, the components and test equipment.

When the project is completed, testing of the complete system should take place but only for the conditions likely to be encountered in normal operation. It should not be tested to destruction. The testing should be fully documented with results being displayed in tables and graphs as appropriate. These tests will enable the candidate to assess the system and identify faults and limitations. The candidate should aim to modify the final system to correct for any limitations and then produce a final set of performance figures for the completed system. The candidate should then evaluate the final system against the initial specification and so recommend possible further developments.

Where candidates quote directly from a source, e.g. circuit diagrams or sentences, quotation marks should be used and the reference provided in a foot note at the bottom of the page.

Coursework marking grid

The report **MUST** contains **CLEAR** photographic evidence, a completed cover sheet and a Record of Supervision.

A	AIM			
	The candidate:-	(a)	defined the problem to be solved with minimal guidance. Expect **most** to gain this - beware centres which limit choice of possible projects	✓
B	**RESEARCH**			
	The candidate:-	(a)	carried out research from **two** or more named sources. Research on the problem. Magazines, Catalogues, (page numbers) Internet sites (URL). Sources must be given.	
		(b)	carried out investigations of **two** or more relevant factors. e.g. loudness of alarm, time to boil egg, frequency response of ear etc Does not have to be practical - allow research into specific, fundamental components e.g. best type of microphone etc for specific application. Detailed sources must be given.	
C	**SPECIFICATION**			
	The candidate:-	(a)	gave a detailed description of the system requirements specifying at least one parameter. Description of what it is to do, including a qualitative parameter, e.g. it must use blue LEDs!	
		(b)	specified at least one numerical parameter. e.g. Range of supply voltages. Allow if just give a specific value e.g. 9V	
		(c)	specified **numerically** and **realistically** three or more parameters. e.g. Range of supply voltages, current plus one other! Expect good specification if this mark awarded. Expect range of supply voltages etc if this awarded e.g. 7V to 9V. Current, Voltage and Power not acceptable as three parameters.	
D	**GENERATION OF POSSIBLE SOLUTIONS**			
	The candidate:-	(a)	considered more than one solution in outline.❊ Can be a single subsystem so long as an alternative considered. **Beware** those who have 'Pressure pad alarm' as title and then consider IR beams as an alternative!	

	(b)	gave some reasons for the choice of solution. ✺ e.g. cost, implementation, effectiveness etc	

E   SUB-SYSTEM DEVELOPMENT

The candidate:-	(a)	developed the system using subsystems. ✺ Individual subsystems should be identified: Expect to see a System diagram. If not then there should be clear evidence that separate sub-systems have been built and tested as part of the work	
	(b)	performed at least one relevant calculation on a subsystem. ✺ A simple Ohm's law type calculation will do. Beware reverse calculations - AOT and then justify the value. Truth tables can be accepted for this mark if nothing else. Can allow if done empirically and then verified.	
	(c)	devised circuit details of at least one subsystem with minimal guidance. ✺ Minimal guidance refers to that of supervisor, technician, family etc. Text books and support books OK, magazines with component values - you need to be satisfied that some design has taken place.	
	(d)	made and recorded measurements on at least **one** subsystem. More than **one** measurement. Each sub-system should be tested separately. Must be real measurements not Croc Clips measurements. May be located near end of report.	
	(e)	assessed the performance of at least **one** subsystem. Each sub-system should be assessed separately. How well do they work.	
	(f)	considered the interfacing between subsystems. Must be evidence of realistic interfacing issue and some reasons given for action taken. e.g. resistance matching, voltage matching, fan-out, MOSFET to interface to logic gate etc. Look for one example.	

F   SYSTEM DETAILS

The candidate:-	(a)	gave a **clear** description of how the system works. Does not have to be the complete system for this mark - allow omissions. Expect prose.	

	(b)	gave a **clear** and detailed description of how the **complete** system works.� Should be succinct and cover the complete system. Expect prose.	
	(c)	performed at least one relevant calculation on the complete system.✻ If really desperate calculate power consumption! Expect gain for amplifiers etc.	

G	**COMPONENT LAYOUT**		
The candidate:-	(a)	produced a circuit board layout. This refers to the process and can include a little assistance. Not allowed if layout from magazine etc.	
	(b)	produced a well organised circuit board layout with minimal guidance. A witness statement and/or photograph will provide evidence. Again process. Not allowed if layout from magazine etc.	

H	**CONSTRUCTION**		
The candidate:-	(a)	worked safely at all times. A Risk Assessment will provide evidence as will a witness statement.	
	(b)	constructed two or more subsystems of the complete electronic system. They do not have to work for this mark.	
	(c)	produced a neat and well organised electronic system. Photographic evidence, component layout diagram etc. This mark is for neatness.	
	(d)	made part of the system function. A part of the system must do something for this mark a little assistance.	
	(e)	made most of the system function. Can including a little assistance.	
	(f)	made all of the system function **with minimal** guidance. The candidate basically makes the whole system function on his/her own. May often not be awarded.	

I	**TESTING THE SYSTEM**		
The candidate:-	(a)	devised an appropriate test procedure for the complete system. Including a little assistance. Needs to be done BEFORE the testing occurs!	
	(b)	devised a full and appropriate test procedure with minimal guidance for the complete system. The candidate basically devises the whole system tests on his/her own.	

J	**MEASUREMENTS**		

The candidate:-	(a)	made and recorded basic numerical measurements on the complete system. The WHOLE system must be complete and work to some extent for this mark. Allow if whole system can be powered but does not **fully** function. Beware calculations that look like measurements. Measurements must be taken from circuit not Croc Clips etc.	
	(b)	made and recorded **detailed** numerical measurements on the complete system. The WHOLE system must be complete and work (including software) to some extent for this mark.	
	(c)	made and recorded **all reasonable** numerical measurements on the complete system. The WHOLE system must be complete and work (including software) to some extent for this mark.	

K   ASSESSING

The candidate:-	(a)	made some assessment of the overall performance of the complete system. BASIC statements about how well the WHOLE system is functioning. System must be complete and capable of being powered, for this mark.	
	(b)	assessed the working parts of the complete system and referred to the measurements made. DETAILED statements about how well the working parts of the WHOLE system are functioning. System must be complete and capable of being powered, for this mark.	

L   LIMITATIONS AND MODIFICATIONS

The candidate:-	(a)	identified some limitations in the performance of the complete system.❅ The WHOLE system must be complete and work to some extent for this mark. Not sufficient to say it does not work! Must be real limitations - eg swapping 2 x 555 for a 556 or adding an ON/OFF switch is not acceptable.	
	(b)	suggested modifications to overcome the limitations in the performance of the complete system.❅ The WHOLE system must be complete and work to some extent for this mark. Modifications to be made to improve the performance of the COMPLETE system, not individual subsystems to make it work. eg do not allow the repair of one subsystem in order to make the complete system function.	

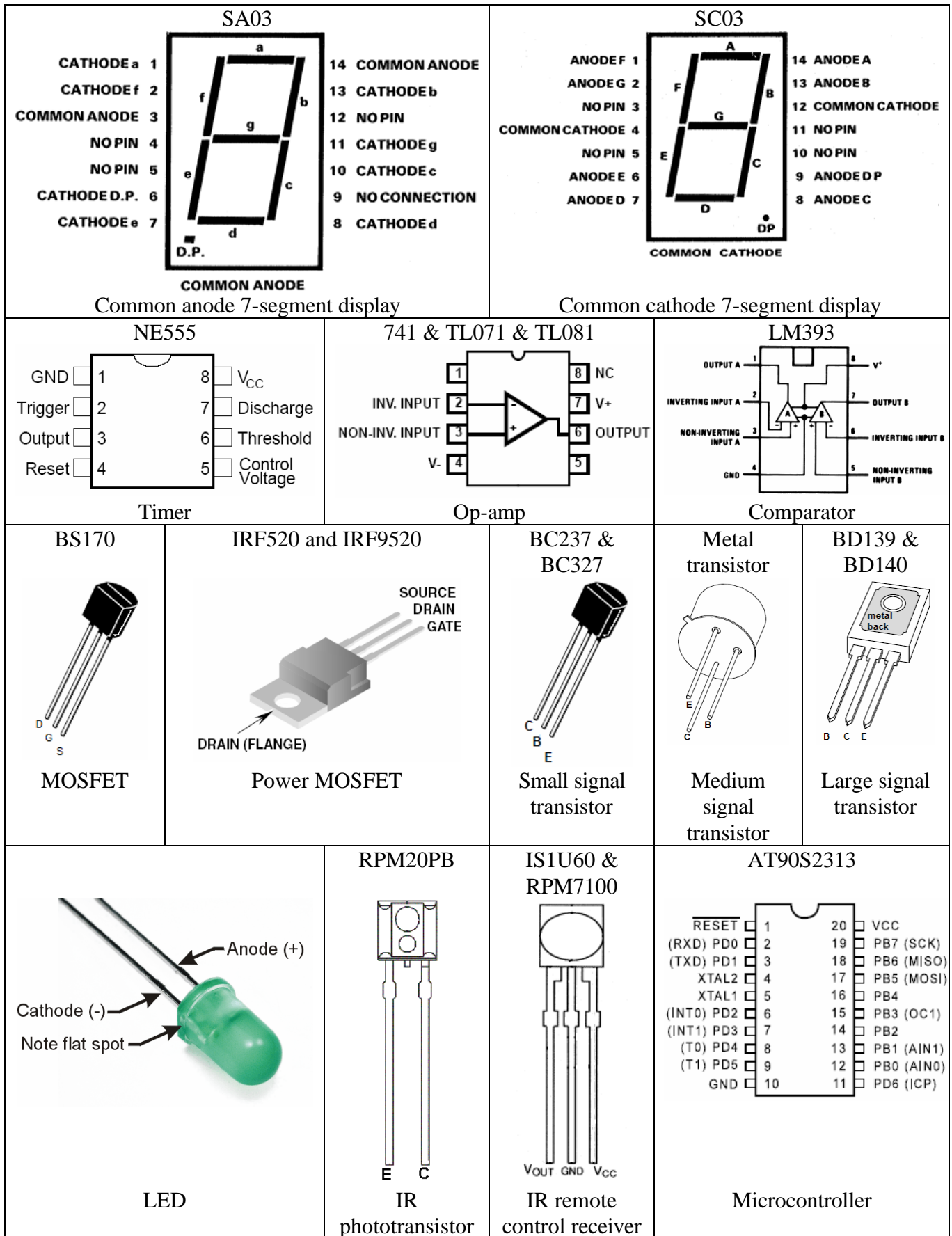|			
	(c)	carried out the modifications. ❋ The WHOLE system must be complete and work to some extent for this mark. Modifications made to the COMPLETE system and need to be more than just making it work! If system perfect then award these three marks but only if Cc has been awarded. Can award if supervisor suggests modification but candidate carries it out.	

M	EVALUATION OF FINAL SYSTEM		
	(a)	The candidate evaluated the performance of the final system against the initial specification. The WHOLE system must be complete and work to some extent for this mark. The final complete system (is retested and) performance is evaluated by comparison with initial specification. Must be numerical.	
	(b)	The initial specifications and final performance agree very closely. The final performance must agree with or exceed the initial specification. Only award if Cc awarded. Must be numerical.	

N	REPORT		
The report:-	(a)	contains a **clear** account of most stages of the development of the project. Detailed and succinct, minor omissions allowed for this mark.	
	(b)	adequately covers all stages of the development of the project. The report needs to chart the development of the project. Complete circuit diagram needed (in some form) for this mark.	
	(c)	contains an acknowledgement of **all** sources of information and help. Candidates need to be aware of penalties for plagiarism!!	

APPENDIX G

74xx00	74xx02	74xx04
NAND gate	NOR gate	NOT gate
74xx08	74xx14	74xx32
Quad AND gate	Hex Schmitt NOT gate	Quad OR gate
74xx47	74xx74	74xx85
LT – lamp test BI/RBO – blanking input/ripple blanking output RBI – ripple blanking input BCD to 7-segment display	Dual D-type flip-flop	4-bit magnitude comparator
74xx86	74xx93	74xx164
Quad XOR gate	4-bit counter	Shift register (serial to parallel)
74xx165	74xx175	74xx193
Shift register (parallel to serial)	4-bit latch	Synchronous counter

SA03	SC03
CATHODE a 1 14 COMMON ANODE CATHODE f 2 13 CATHODE b COMMON ANODE 3 12 NO PIN NO PIN 4 11 CATHODE g NO PIN 5 10 CATHODE c CATHODE D.P. 6 9 NO CONNECTION CATHODE e 7 8 CATHODE d D.P. COMMON ANODE	ANODE F 1 14 ANODE A ANODE G 2 13 ANODE B NO PIN 3 12 COMMON CATHODE COMMON CATHODE 4 11 NO PIN NO PIN 5 10 NO PIN ANODE E 6 9 ANODE D P ANODE D 7 8 ANODE C DP COMMON CATHODE
Common anode 7-segment display	Common cathode 7-segment display

NE555	741 & TL071 & TL081	LM393
GND 1 8 V$_{CC}$ Trigger 2 7 Discharge Output 3 6 Threshold Reset 4 5 Control Voltage	1 8 NC INV. INPUT 2 7 V+ NON-INV. INPUT 3 6 OUTPUT V- 4 5	OUTPUT A 1 8 V+ INVERTING INPUT A 2 7 OUTPUT B NON-INVERTING INPUT A 3 6 INVERTING INPUT B GND 4 5 NON-INVERTING INPUT B
Timer	Op-amp	Comparator

BS170	IRF520 and IRF9520	BC237 & BC327	Metal transistor	BD139 & BD140
D G S	SOURCE DRAIN GATE DRAIN (FLANGE)	C B E	E C B	B C E metal back
MOSFET	Power MOSFET	Small signal transistor	Medium signal transistor	Large signal transistor

LED	RPM20PB	IS1U60 & RPM7100	AT90S2313
Anode (+) Cathode (-) Note flat spot	E C	V$_{OUT}$ GND V$_{CC}$	$\overline{RESET}$ 1 20 VCC (RXD) PD0 2 19 PB7 (SCK) (TXD) PD1 3 18 PB6 (MISO) XTAL2 4 17 PB5 (MOSI) XTAL1 5 16 PB4 (INT0) PD2 6 15 PB3 (OC1) (INT1) PD3 7 14 PB2 (T0) PD4 8 13 PB1 (AIN1) (T1) PD5 9 12 PB0 (AIN0) GND 10 11 PD6 (ICP)
LED	IR phototransistor	IR remote control receiver	Microcontroller