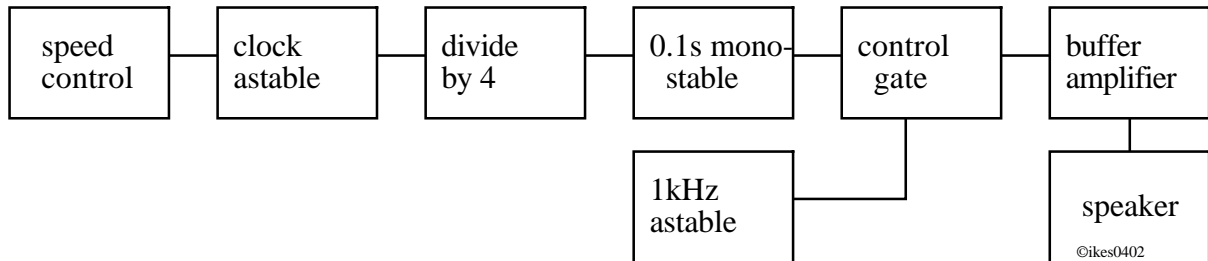


## Counter, Timer and Logic revision.

- 1). A metronome is required that has a speed range from 15 beats per minute up to 240 beats per minute, each beat being marked by a short tone pulse of 1000Hz and duration 0.1s. A proposed system diagram is shown below.

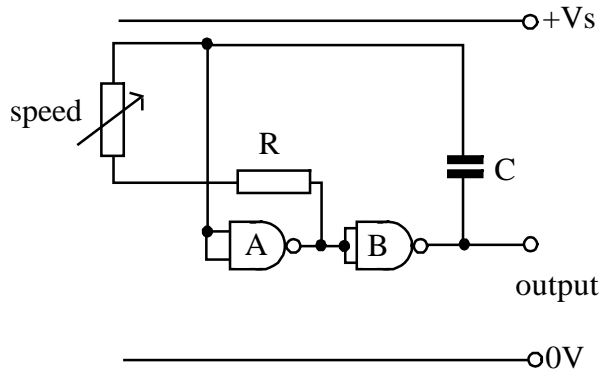


- (a) (i) The clock astable is to be made from NAND gates. Complete the truth table for a two input NAND gate, shown below.

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

(1)

- (ii) The circuit diagram for a NAND gate astable is shown below.



By referring to the circuit diagram, explain how a NAND gate astable operates.

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(5)

(iii) Explain why the maximum value for C tends to be  $1\mu\text{F}$ .

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(2)

(iv) The slowest speed of the metronome is 15 beats per minute. What is the frequency of the beats?

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(1)

(v) By referring to the system diagram, state the frequency of the astable needed to give this metronome speed.

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(1)

(vi) If C has a value of  $1\mu\text{F}$ , calculate the combined resistance of the variable resistor and the fixed resistor R to give this frequency.

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(2)

(vii) The fastest speed of the metronome is 240 beats per minute. What is the frequency of the beats?

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(1)

(viii) By referring to the system diagram, state the frequency of the astable needed to give this metronome speed.

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(1)

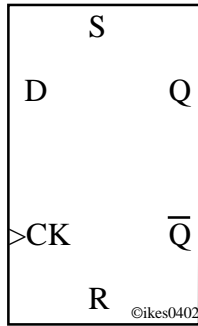
(ix) If C has a value of  $1\mu\text{F}$ , calculate the resistance of the fixed resistor R to give this frequency.

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(2)

- (b) The divide by 4 circuit is made from two D-type flip-flops. The circuit symbol for a D-type flip flop is shown below.



- (i) Explain the meaning of each of the labelled connections.

S .....

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D .....

.....

CK .....

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R .....

.....

Q .....

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- (ii) Explain how a D-type flip-flop functions

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- (iii) Draw in the space below the circuit diagram for the divide by 4 counter.

(5)

(2)

(4)

- (c) (i) The 0.1s monostable is made from NAND gates. In the space below draw a labelled circuit diagram of a NAND gate monostable clearly showing the input and the output.

(4)

- (ii) Explain how the NAND gate monostable functions.

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(5)

- (iii) If the timing capacitor used in the monostable is 100nF, calculate a suitable value for the timing resistor.

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(2)

- (iv) During the timing period, what is the logic state of the output of the NAND gate monostable?

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(1)

- (d) The 1kHz tone is generated by another NAND gate astable.
  - (i) In the space below, draw the circuit diagram of a NAND gate astable (without looking back to part (a)!).

(3)

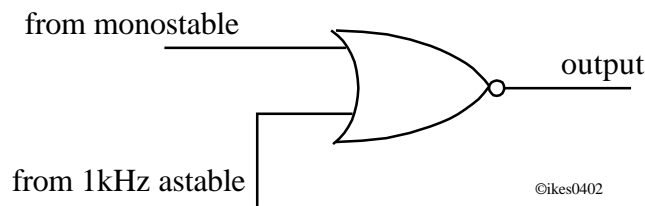
- (ii) Calculate suitable component values to give a frequency of 1kHz.

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(2)

- (iii) By considering your answer to part (c)(iv), explain how the circuit diagram below will enable 0.1s pulses of 1kHz frequency to be produced.



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(2)

- (e) The output from the circuit above produced a very quiet sound when connected directly to a loudspeaker.
  - (i) Draw in the space below the circuit diagram of a MOSFET buffer that can be used to interface the output of the NOR gate to a loudspeaker.

(3)

(ii) State three properties of a MOSFET that make it suitable for this application.

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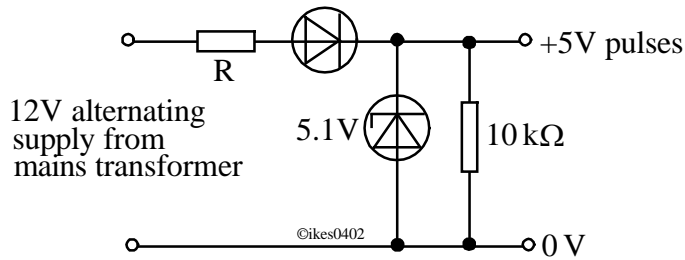
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(3)

2). A student wants to construct a circuit that produced pulses of 1 second. He decides to use the mains as a frequency reference and constructs the following circuit to produce pulses of approximately 5V amplitude and frequency 50Hz from a 12V alternating supply.



(a) (i) Explain why the output consists of pulses at a frequency of 50Hz.

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(1)

(ii) What is the period of the pulses?

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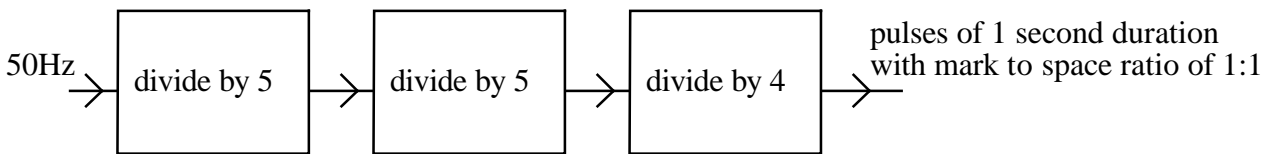
(1)

(iii) Explain why the pulses have an amplitude of approximately 5V.

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(3)

(b) The system diagram below shows how the 50Hz pulses are converted into 1 second pulses.

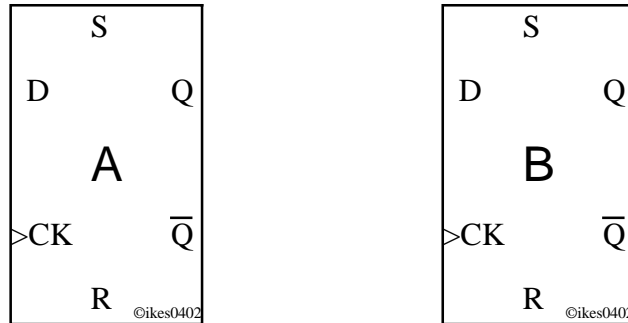


(i) Explain what is meant by the term mark to space ratio.

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(1)

- (ii) The diagram below shows two rising edge triggered D-type flip-flops. Complete the circuit diagram below to show how they can be connected to form a divide by four up-counter. Label the input and the output.



- (iv) Explain how this circuit functions. (5)

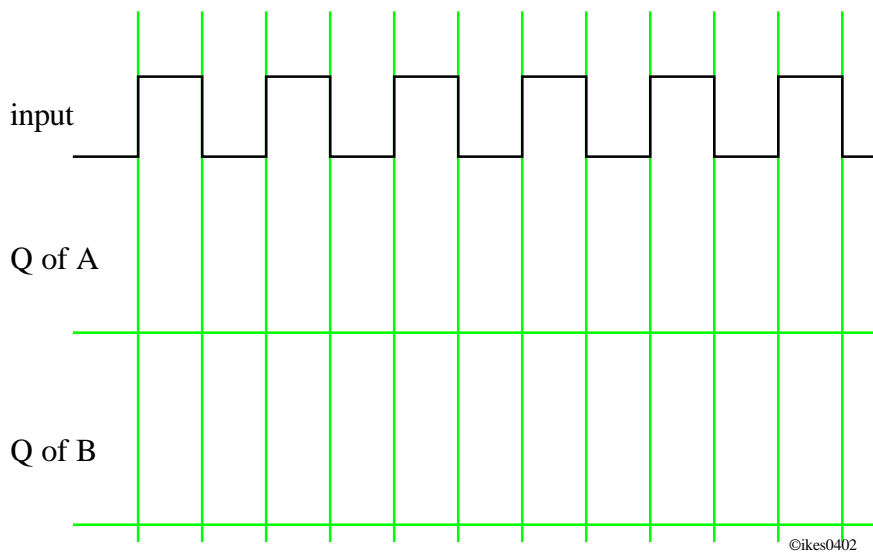
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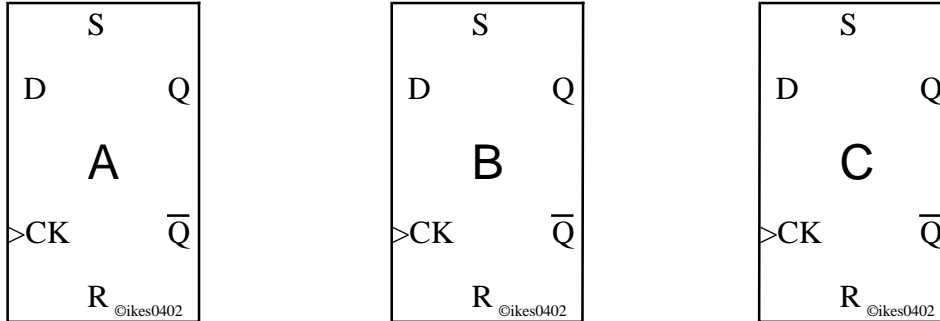
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- (v) Complete the timing diagram below for the Q output of A and the Q output of B. (3)



- (c) The diagram below shows three rising edge triggered D-type flip-flops.
- (i) Using any additional components that you require, complete the circuit diagram to show how they can be connected to form a divide by five up-counter. Label the input and the output.



(5)

- (ii) Explain how this circuit functions.

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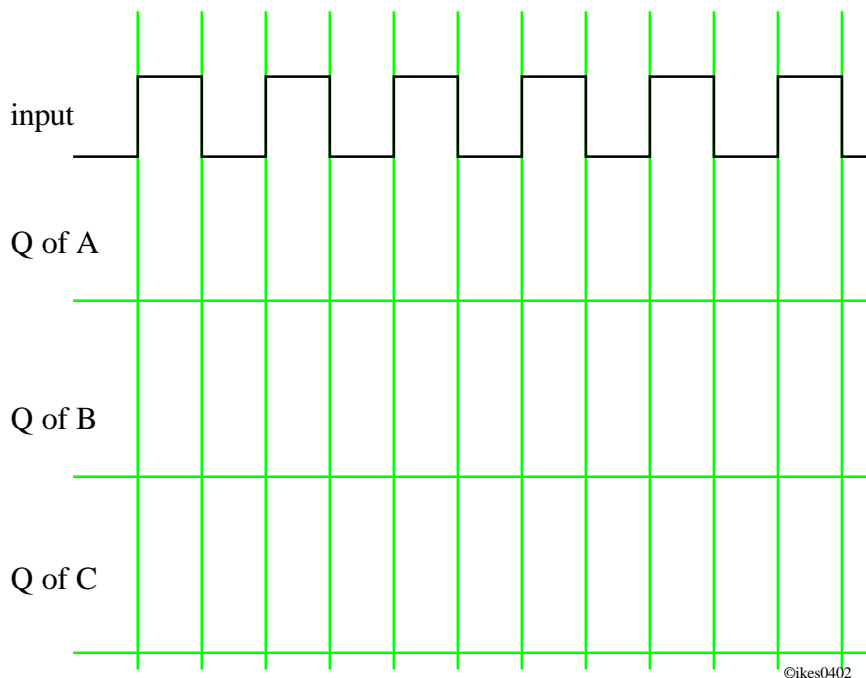
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(3)

- (iii) Complete the timing diagram below for the Q outputs of A, B and C.



(4)

3). As part of a game for a fair, a display board is required that has 4 lights flashing in sequence, in a square, at the edge of the board. A student is asked to construct this lights effect and decides to use a four bit shift register.

(a) Explain what is a shift register.

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(1)

(b) The shift register is to be constructed from *rising edge triggered D-type flip-flops*. Explain the meaning of the following terms:

(i) rising edge triggered,

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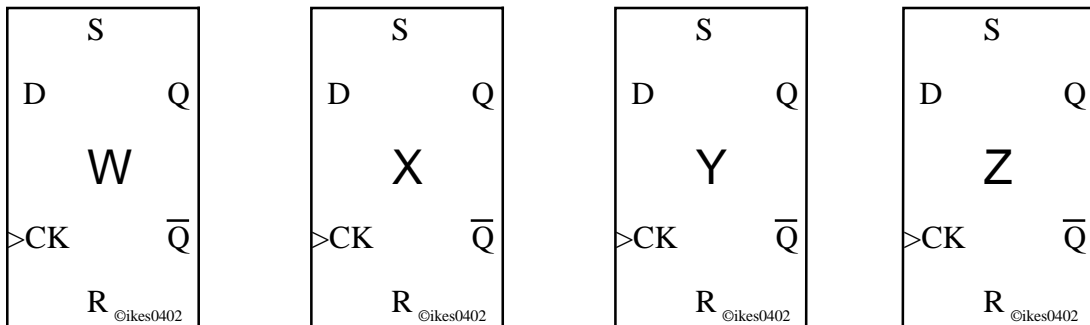
(1)

(ii) D-type flip-flop.

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(1)

(c) Complete the circuit diagram below to show how the four D-type flip-flops are connected to form a suitable shift register. Label the clock input and the serial data input.



(5)

(d) A 12V 24W lamp is to be connected to each Q output via a buffer circuit.

(i) Explain why the buffer circuit is needed.

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(1)

- (ii) A transistor or a MOSFET could be used as the buffer. State three reasons why a MOSFET is more suited to this application.

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(3)

- (iii) Draw below the circuit diagram of a MOSFET buffer for this application.

- (d) Only one lamp is to be lit at any time and so the student sets up a truth table for the serial data input as shown below. (3)

Data input (D)	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
1	0	0	0	1
0	1	0	0	0
0	0	1	0	0
0	0	0	1	0

- (i) State the Boolean expression for D.

.....

(1)

- (ii) Draw below a circuit diagram to implement this expression, labelling the inputs and output.

(3)